Investigation of RLCK-Extraction

CONTENTS

1 TIME OVERVIEW

A brief overview of the work activities during this internship is given in Tab. 1.

2 REPORT

2.1 INTRODUCTION

2.1.1 MOTIVATION FOR PARASITIC EXTRACTION

In the design of integrated circuits, parasitic elements are circuit components – mostly resistors, inductors capacitors – which are, in most cases, not desirable for for the purpose of the circuit. These elements do not appear in the initial schematic of an electrical network created by the circuit designer, they are only a result of its layout. In other words, the physical placement of the primitive devices (transistors, etc...) will result in these unwanted circuit elements, and they can affect the functionality of the design.

In highly integrated circuits parasitic effects are almost always relevant. If they are not considered in the design phase carefully they can lead to malfunctions of the IC. For example, they can affect signal integrity in terms of delay variations, overshoots, oscillations and rise time degredations. With operating frequencies approaching the gigahertz range, the extraction of parasitic inductances is becoming increasingly relevant in the design and analysis of on-chip interconnect [1]. Inductances and resistances can also adversely affect power integrity, and can, for instance, cause malfunctions of internal voltage regulators. This may cause the entire chip to crash [2].

An increasing desire for cheaper and faster design cycles of chips driven by high demands and a highly competitive market has boosted the importance of first-time silicon correctness. An extremely important step in achieving to produce fully functional chips in the first design cycle is the control of harmful parasitic effects within the IC. Therefore, accurate parasitic extraction plays an essential role for pre-silicon verification.

2.1.2 EXTRACTION OF INDUCTANCES

Unlike parasitic capacitances where only nearest neighbours are required to be taken into account, the extraction of parasitic inductances is more expensive since limiting the extraction to nearest neighbour couplings would yield inaccurate results [2]. Due to the inductance being a function of a closed loop current path, it is required that a return current path in 3D-space is constructed for each conductor segment. This is internally performed by the tool and not visible to the user. The space enclosed by this return current is the region where inductive couplings can occur [2].

We use the so-called Partial Element Equivalent Circuit (PEEC) method to extract inductances. The implementation we use is the one provided by QRC in RLCK mode. The resultant system of equations in the SPICE-solver of the obtained circuit is similar to a boundary element method discretization of the currents and charge density where Maxwell's equation is the PDE to be solved. Thus, we can think of the parasitic circuit as a boundary representation of Maxwell's equations in matter using adequate Green's functions and a suitable problem adapted set of basis-functions. The equations resulting from such a boundary-discretization can always be either interpreted in terms of the field-solution or in terms of circuit elements (capacitors, resistors, inductors and ind. couplings) written in the form of an electrical circuit [3]. The exact choice of basis functions, the meshing algorithm and further

Work Activity	Calendar Week
Introduction to industrial RF engineering	7 - 8
RF characterisation of our test structures on the wafer level	9 - 11
Introduction to automatic data processing using Python and SPICE-class circuit simulators	12 - 14
Verification and optimization of data processing routines	15 - 17
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Data processing, parameter extraction, evaluation of measured data	22 - 25
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Documentation	30 - 31

Tab. 1 | Time overview of the work activities during the internship.

approximations are proprietary knowledge of tool vendors. If no distance limit is applied to the inductive couplings, then the result is a dense partial inductance matrix. This will often overwhelm circuit simulators in terms of memory usage or require far too long simulation times to be used in practice. For example, full-chip extraction of chips with digital interconnects is, thus, rather difficult [2]. Therefore, the tool must sparsify the inductance matrix based on reasonable approximations. It is difficult to find criteria to sparsify an inductance matrix that can be universally applied. An example criterion could be to set couplings beyond a certain cutoff radius to zero. However, tool vendors usually do not fully disclose the approximations used for sparsification in order to protect their intellectual property from competitors. Figure 1 gives a rough overview on how PEEC-based RLCK extraction can be categorized among the finite- and boundary element method.

2.1.3 THERORETICAL BACKGROUND

This section briefly details the theory tied to the experimental content of this report. A description n-port network parameters and de-embedding is given. Moreover, SPICE-class netlists and touchstone files are introduced, and finally the procedure of measuring S-parameters is described.

Ports A port of an electrical network is defined as a pair of terminals that satisfy the so-called port condition: The port condition requires the two terminals to have equal but opposite current flowing through them. In microwave topologies that have multiple ports, such as transmission lines, the second terminal of each port are internally shortend. This node common to all ports is usually identified as “ground”. The definition of ports allows for an electrical network to be regarded as a “black box” which means that rather than representing it by circuit elements, we define its behaviour using its network parameters [4].

Network Parameters The small signal response to any n-port network (= electrical network with n ports) is fully defined by a frequency-dependant $(n \times n)$-matrix (complex-valued). There are multiple conventions for this complex-valued matrix. For networks operating at radio and microwave frequency the scattering parameters (S) are often used. S-parameters relate incident and outgoing power waves relative to some wave guide impedance Z_0 (usually 50Ω) at each port to each other. They can be interpreted as reflection- and transmission coefficients. The S-parameter matrix can be converted to other parameter types which for instance, instead relate currents and voltages at its ports. Examples are Y- and Z-parameters. In the special case of a 1-port network the Z-parameter matrix reduces to the frequency impedance of the network, and the Y-parameter matrix thus to the network’s admittance [4, 5].

De-embedding De-embedding is the act of taking S (Y, Z,...)-parameter obtained from measurement (sometimes simulation) and removing effects caused by components of the network that were not intended to be measured or could not be removed for the simulation. This could be, for instance, capacitances of the pads (see section 2.2.2) which are needed to establish electrical contact with the probe [6].

SPICE-class netlist A netlist is a computer-readable representation of an electrical circuit, and, on the most fundamental level, consists of “nodes” and “devices”. Devices such as resistors, inductors, transistors etc. connect nodes. A SPICE-class netlist is a file format that can be simulated using SPICE-class circuit simulators. Each line of a SPICE file format netlist contains the name and specifications of an electrical device and the names of the nodes to which it is connected. Ports are a type of device and can be instantiated using previously defined nodes. Using a special simulation mode, we can obtain S-parameter data in the same format as written by VNAs (touchstone). Below, a short example of an S-parameter simulation of a network consisting of two coupled inductors and a resistor is shown [7]:

```
*comment after ";" or "*"
L1 node1 node2 1e-9 ; inductor con. node1
    and node2 with 1nH
R1 node2 node3 1e-2
L2 node3 node4 1e-9
K12 L1 L2 K=.5
.CONNECT node4 0; connecting node3 to ground
    (0).
VP0  node0 node3 PORT R=50 DC 0
*VP0 defines a port between node0 and node3
.AC  DEC  20 100k 10G
.SPARAM VP0; S-parameter sim from 100kHz to 1
    0GHz
.SAVE inductive_coupling_touchstone
.END
```

Touchstone File Touchstone is a machine-readable file format for network-parameters. The output of the netlist above is a so-called touchstone file. A touchstone file contains S-parameter (sometimes Y-parameter) values for multiple frequency points. It is an industry standard for circuit simulators and measurement equipment (e.g. VNAs). Their file suffix is usually “.sp” or “.snp”, where n is the number of the network’s ports.

Measuring S-parameters An instrument that is typically used to measure the complex S-parameters (amplitude and phase) of an electrical network is a Vector Network Analyser (VNA). We use a model manufactured by Keysight, which allows for measure-

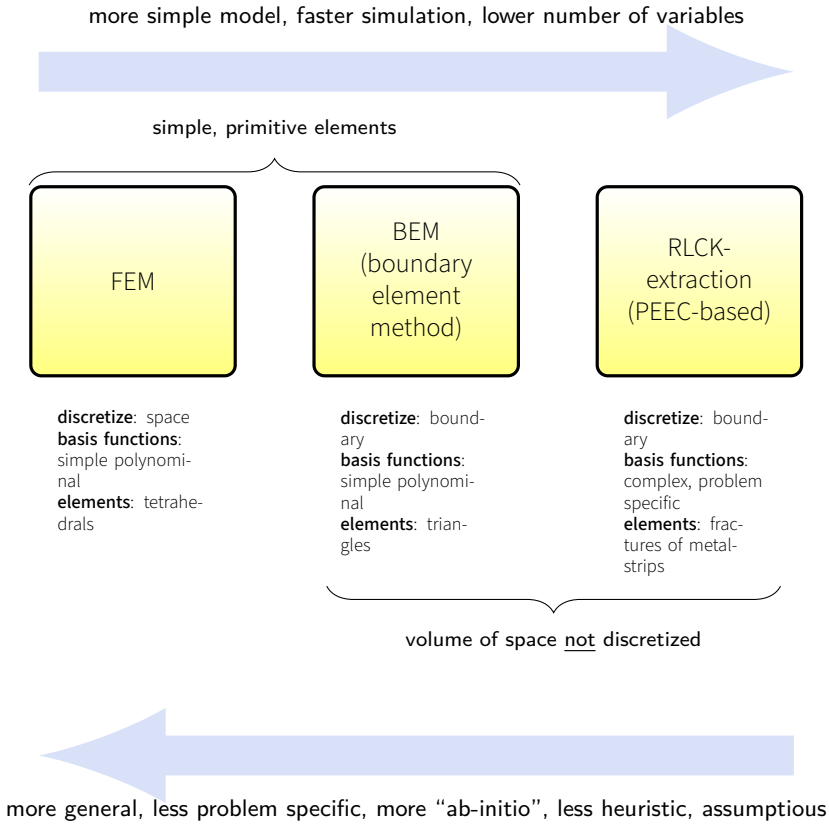

Fig. 1 | Overview of some numerical PDE solving methods. Comparison of finite element method, boundary element method and PEEC-based RLCK extraction.

ments at up to 8.5 gigahertz. Given the size of the structures to be measured (see section 2.2.1) special equipment is needed to establish a stable and well-defined electrical connection between the VNA and our structures. another important requirement is that the terminals connected to the ground-shield of the coaxial cables are connected on the wafer. To establish such a connection we use HF wafer-probers that are connected to the end of a high quality coaxial cable. These probers consist of very small tips (different pitches and pin-orders e.g. GS, GSG[1] are commercially available). We use probers with a pitch smaller than 150µm between signal and ground tip. A crucial part of any VNA measurement is calibration. In order to achieve a good calibration the VNA has to be warmed up for at least 1 hour. Then, depending on what type of measurements (eg. 1-port or 2-port) are to be carried out, and depending on the wafer prober and frequency range multiple calibration-measurements on a special calibration substrate have to be performed. 2-port calibration usually requires measurements of four known standards called short, open, load, thru (SOLT). In contrast, a 1-port calibration only requires short, open load. Raw data (i.e.without a calibration) is practically useless since the structure is electrically smaller than effects caused by cables and connectors by orders of magnitude. Therefore, calibration is vital to obtain accurate data [6].

2.1.4 VALIDATING QRC'S RLCK-EXTRACTION USING MEASUREMENTS AND FINITE ELEMENT SIMULATION

This report briefly presents some results from our evaluation of Quantus QRC an extraction tool by Cadence. While QRC offers an RC extraction mode which is predominantly used for applications in which capacitances play an important role (e.g. ring oscillator circuits), it also offers a more advanced RCLK extraction mode. In addition to resistances (R) and capacitances (C), RCLK extraction will also extract inductances (L) and inductive couplings (K). QRC's RLCK extraction uses, according to its user manual, an implementation of the PEEC method. However, many details of this implementation are not disclosed, and, using the documentation alone, it is difficult to estimate whether QRC's implementation is adequate for a certain application.

In previous work, a test wafer with inductive test structures has been manufactured. Among others, we apply QRC's RLCK extraction to a layout consisting of a series of loop-shaped structures that can be found on our wafer. Then we compare the results with our measurements. S-parameters of the loops are simulated from the QRC output using SPECTRE – a SPICE-compatible circuit simulator by Cadence. A Python-routine then fits an RL-model to the Z-parameters of each network. Finally, the resulting fit-parameters of the simulation are compared with measurement as well as with simulation data obtained from Ansys HFSS[2]. All S-paramter data sets are fitted to the same RL-model using the same routines.

2.2 FOCUS OF THIS REPORT —RCLK EXTRACTION

2.2.1 LOOP SHAPES AND FRACTURING

Among others, the accuracy of L and K extraction of QRC is evaluated using a series of loops that have a fixed circumference but

[1] G: ground, S: signal

[2] HFSS is a finite element field solver. HFSS data was obtained by simulating every loop seperately.

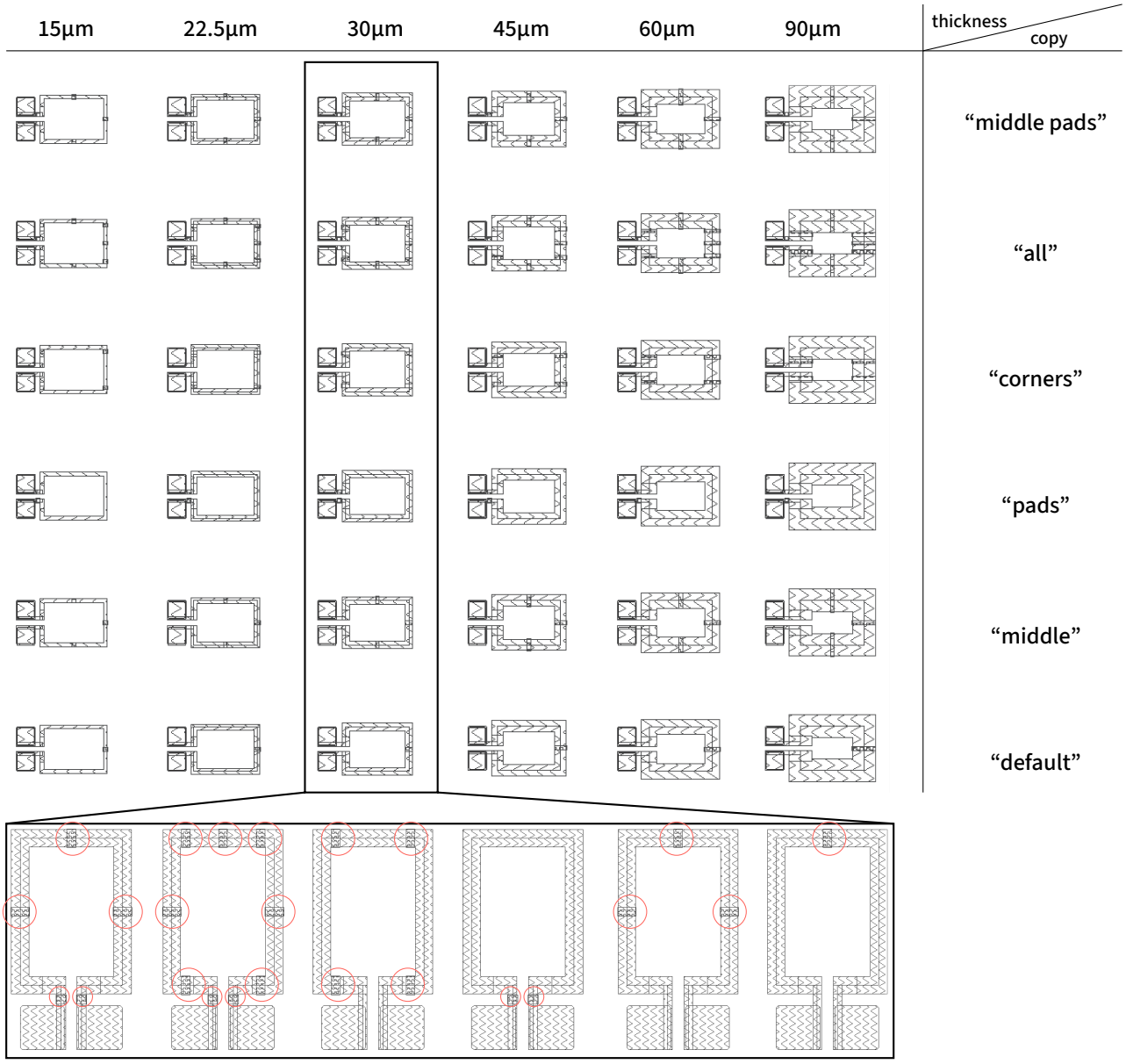

Fig. 2 | QRC test layout. Layout contains loop-structures for QRC featuring variations of loop thickness and resistor patch placement. A Close-up view of every resistor placement pattern can be seen in the bottom box. Resistors are indicated by red circles.

differ in wire thickness. There are six different thickness levels ranging from 15µm to 90µm. Simple loop-shaped structures show predictable inductive behaviour and can be calculated using simple textbook formulas (see section 2.2.2). Thus, they serve as a most simple test case.

The number and position of fractures QRC uses for a loop can, to some degree, be controlled using patches of resistors (Figure 2, *bottom*). Here, the term *fracture* refers to a piece of lengthy metal strip automatically created by QRC. Electrically, each fracture corresponds to a node connected by parasitic Rs, Ls, and Cs whose value is automatically computed by QRC. Our resistor patches were placed on top of the loop wire in areas where we intend to enforce a fracture. QRC then automatically adds additional fractures by some, not fully documented, heuristic. In “default” mode QRC seems to split every strip separated by resistor patches into two parts except if a strip is longer than 200µm: In this case, the strip is subdivided until each fracture is smaller than 200µm. Fractures are often angled. To evaluate the influence of the fracture geometry, we created six different identical copies of the same loops that differ only in the placement of the resistor patches. The copies are named, according to where the resistor patches were placed, as follows: “default”, “middle”, “pad”, “corners”, “all” and “middle pad”. The complete layout of the loop-shaped structures with resistor patches is shown in Figure 2. Figure 3 shows the fractures which QRC generated for every copy of every loop in this layout .

2.2.2 FITTING OF THE S-PARAMETER DATA USING A PYTHON-ROUTINE

A simple RL-model consisting of a series resistance and a series inductor is assumed (Figure 4) of which “L” is of primary interest.

$$Z(\omega) = R + i\omega L \tag{1}$$

The real part of the Z-parameter is constant and the imaginary part is linear in frequency. Figure 6 shows that this simple model is indeed sufficient to fit the QRC-simulation data. We have seen that it can also fit the imaginary part of our measurement data

Fig. 3 | Fractures for every loop generated by QRC.

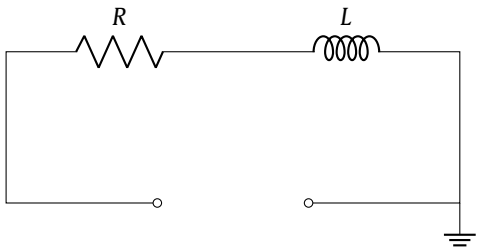

Fig. 4 | Topology representing the simple RL-fit model

– and hence the total in inductance can be obtained (Figure 6). However, it is not sufficiently good enough for HF measurement data for the real part. In section 2.2.3, a more elaborate model is introduced which is used to fit the measured data in the whole frequency domain.

Our Python-routine fits this model to the data obtained from QRC. Before fitting this model the S-parameters from the touchstone file first have to be to converted to Z-parameters. We use the Python-library Scikit-rf [8] to read and process touchstone files. Scikit-rf can create "Network" objects from touchstone files which provide functions to convert the S-parameters to any other common form including Z, Y and ABCD-parameters. Using this library has proved to be particularly useful as it strongly reduces the work spent with programming, and it was found to be well-tested, well-documented, actively maintained and feature-rich. The simplicity of use is demonstrated by the very short and intuitive code below:

```
# pseudo-code
import skrf as rf # importing Scikit-rf
netw = rf.Network("/data_dir/touchstone.s1p")
z_params = netw.z # array containing
    Z-parameters
y_params = netw.y # array containing
    Y-parameters
```

Another important step before fitting the loop data is to remove the influence of the pads. To do this, we use special "short" and "open" de-embedding structures, that are also simulated by QRC + SPECTRE, HFSS, and which were also measured. Figure 5 shows these structures along with the circuit elements they cause.

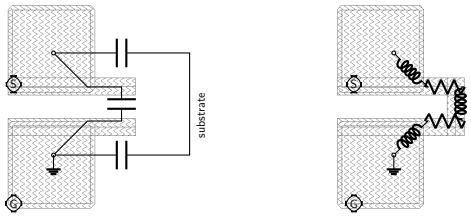

Fig. 5 | De-embedding structures open (left) and short (right).

The circuit topology assumed for the "open"-structure (Figure 5 *left*) consisting of parallel capacitors can be simplified to an overall capacitance between signal (S) and ground (G). Therefore the Y-parameter of this structure can be assumed to have the following form:

$$Y(\omega) = i\omega C \tag{2}$$

To extract the value of C, the above model is fitted to the Y-parameter curve of the "open"-structure. The same capacitance also occurs in the measured and simulated loops and is parallel to the loop to be measured. De-embedding this capacitance C therefore boils down to the following formula:

$$Y_{\text{deembed}}(\omega) = Y_{\text{sim/meas}}(\omega) - i\omega C_{\text{open, sim/meas}} \tag{3}$$

It is worth mentioning that the effect of removing the capacitance was negligibly small.

The "short" structure as seen in Fgure 5 (*right*) is used to remove the inductive and resistive impedance of the pads. Here, a simple RL-model is assumed. Since here the impedance to be de-embedded is in series we must subtract it from the Z-parameter:

$$Z_{\text{deembed}}(\omega) = Z_{\text{sim/meas}}(\omega) - R_{\text{short, sim/meas}} - i\omega L_{\text{short, sim/meas}} \tag{4}$$

By substituting Eq. (3) in to Eq. (4) and using $Y = Z^{-1}$ we obtain our de-embedding rule:

$$\begin{aligned} Z_{\text{deembed}} = & \\ & (Y_{\text{sim/meas}}(\omega) - i\omega C_{\text{open, sim/meas}})^{-1} \\ & - R_{\text{short, sim/meas}} \\ & - i\omega L_{\text{short, sim/meas}} \end{aligned} \tag{5}$$

An exemplary fit plot can be seen in Figure 6.

2.2.3 DE-EMBEDDING AND FITTING OF THE MEASURED DATA

The measured S-parameters are de-embedded and fitted using the same Python-routines used for the QRC-data. In contrast to the QRC generated S-parameter files, the RL-model does not fit the real part in the HF region $f > 1$GHz (see Figure 8)) from section 2.2.2. It was observed that, in the measured data, at high frequencies a drop in the imaginary- and an increase in real impedance occurs. This can be explained by induced loop currents underneath the loop-shaped conductor, which flow in the silicon substrate. They are known as eddy currents. We use a model as seen

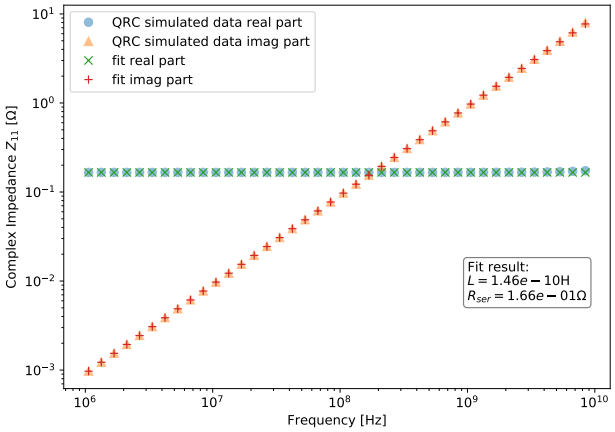

Fig. 6 | Complex-valued impedance Z_{11}. Data obtrained from simulation + de-embedding (circle and triangle) and the RL-fit (Eq. (1), cross and plus) of the loop with wire thickness 15µm (see Figure 2). The simulation used SPECTRE+QRC with the resistor patch configuration "all".

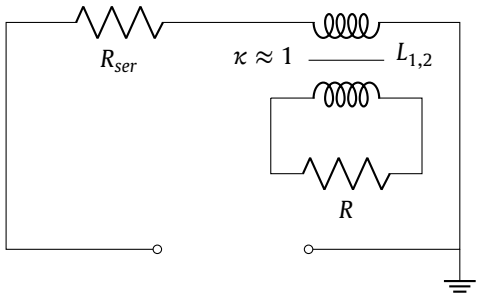

Fig. 7 | Our empirical circuit for loops of metal over a silicon substrate. The inductive coupling and the resistor R_R realize the eddy current loss, and thereby extend the circuit from Figure 4.

in Figure 7 to describe this effect. Using the definition of mutual inductance from [9] the Z-parameter of this network is given by:

$$Z(\omega) = i\omega L + R_{\text{ser}} - \frac{M^2\omega^2}{i\omega L - R} \tag{6}$$

where $M = \kappa\sqrt{L_1 L_2}$. We use $\kappa \approx 1$ and $L_1 \approx L_2 = L$ is assumed. Therefore $M = L$. Since this fixes κ, M and L_2, only L, R_{ser} and R are fitted.

An exemplary fit plot can be seen in Figure 8.

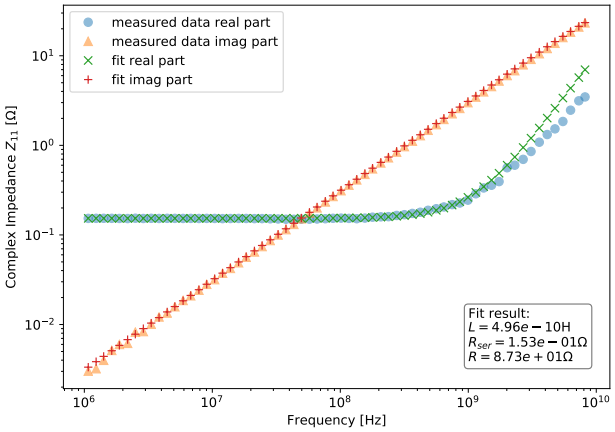

Fig. 8 | Complex-valued impedance Z_{11}. Data obtained from VNA-measurements of loop with wire thickness 15µm (see Figure 2) after de-embedding (circle and triangle) and "Eddy current"-fit (Eq. (6), cross and plus).

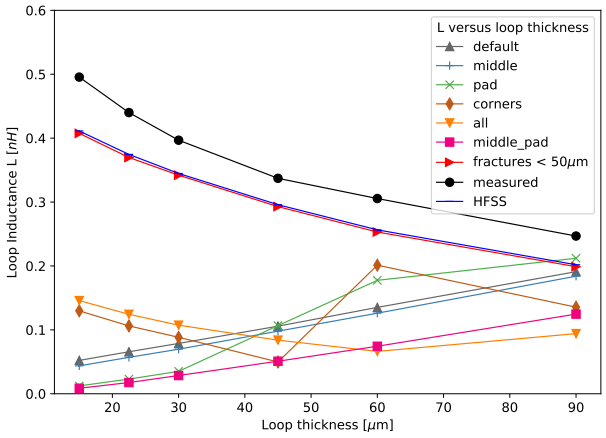

Fig. 9 | Loop inductance. Measured, HFSS-simulation and one curve for each resistor placement configuration simulated with QRC+SPECTRE. Additionally, QRC+SPECTRE simulation with fractures limited to length of 50µm.

2.2.4 COMPARISON OF THE FIT RESULTS

Insight about QRC's capabilities is gained by plotting the extracted inductances obtained through our fitting routines against the loop thickness. Figure 9 shows a curve for each resistor placement pattern in QRC, the curve of the measured data as well as the curve corresponding to HFSS. HFSS data was fitted to the same model as the measured data.

A decrease of overall inductance with increasing thickness is to be expected as a thicker wire allows for the current to take a smaller loop path. This behaviour can be seen in the measured data, and in the data obtained from HFSS. Moreover, the values of the inductances extracted from HFSS data are reasonably close to the measured data. In contrast, all of the QRC data except for the setups "all" and "corners" yield graphs showing an increase in overall inductance with thicker wire. Yet, a tendency of decreasing inductance with thickness is seen in the graphs resulting from the resistor placement patterns "all" and "corners". These setups, "all" and "corners", have more fractures along the shorter axis. This hints at the need of a larger number of shorter, fractures in order to achieve reasonable results. In fact, we have also simulated these structures with fractures limited to be no longer

than 50µm in length, and there we obtained results close to our measured data.

2.2.5 CONCLUSION

The data obtained from our finite elements simulation using Ansys HFSS has, as expected, povided accurate results. This is not true for the data QRC produces from the six different resistor placement patterns we used in this evaluation for our loops. However, each of the data sets yields different results which indicates that fracturing has an impact on the extraction executed by QRC. Indeed, we found that the accuracy is satisfactory if very small fracturing is used. The use of shorter fracures however means that there will be a larger number of fractures, and hence more computation time is required. The fracture size needed for obtaining sufficient accuracy is unreasonably small in case of these loop structures. In sharp contrast, in other measurements of simple transmission lines we found that the number of fractures has little to no impact on the extracted inductance, which is very useful for us as simulation performance is of particular interest. In these TL-structures (which are beyond the scope of this report) the accuracy of QRC was excellent even for a very small number of fractures. This shows that QRC RLCK has probably been optimized and tested only for TL-like structures. It could also mean that we have uncovered a bug, and there is hope that this deficiency is fixed in a future release. It seems that inductive couplings are not calculated correctly by QRC if the fractures are angled or perpendicular, and if the size of the fracture is large with regards to the size of the structure. In fact, we have observed a strong increase in computation time after decreasing the fracture size. Consequently, whole-chip RLCK-extraction simulation is indeed feasible (given only power copper is LK-extracted) but as long as the shortcoming of QRC we uncovered remains the accuracy is limited. However, it should be noted that the test cases in this report are extreme cases and the errors should not be overstated.

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