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„Analysis of Substrate Impedances in BCD-Technologies with different Simulation Techniques“

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Zusammenfassung

In dieser Arbeit wird eine niedrigdimensionale parasitäre Substratschaltung vorgestellt, die nur wenige Kondensatoren und Widerstände enthält, durch die Substratkopplungen zwischen zwei benachbarten Bauelementen auf einem Die, die in der betrachteten BCD-Technologie hergestellt wurden, leicht abgeschätzt werden können. Die Werte der Widerstände, von denen einige von der Frequenz und dem Abstand, um den die beiden Bauelemente getrennt sind, abhängen, werden aus einer 2D-FEM-Simulation eines Substratmodells der BCD-Technologie erhalten. Darüber hinaus gibt eine genaue Analyse der Widerstände in dieser Schaltung einen Einblick in die Substratstrompfade und zeigt auch Einschränkungen hinsichtlich der Genauigkeit von Kopplungsvorhersagen auf, die unter Verwendung dieser Schaltung gemacht werden können. Der Rest dieser Arbeit verwendet die Ergebnisse der 2D-FEM-Simulation, um zwei Substratextraktionstools zu bewerten. Das erste tool ist die QRC Substrate Extraction Solution von Cadence und das zweite Werkzeug ist ein in-house entwickeltes Substratextraktionswerkzeug.

Abstract

In this thesis, a low dimensional parasitic substrate circuit – containing few capacitors and resistors – is presented through which substrate couplings between two adjacent devices on a die, fabricated in the considered BCD technology, can easily be estimated. The values of the resistors, some of which are dependant on frequency and the distance by which the two devices are separated, are obtained from a 2D FEM simulation of a substrate model of the BCD technology. Moreover, a close analysis of the resistors in this circuit gives some insight into substrate current paths and also reveals limitations regarding the accuracy of coupling predictions that can be made using this circuit. The remainder of this thesis uses the the results from the 2D FEM simulation to evaluate two substrate extraction tools. The first tool is the QRC substrate extraction solution by Cadence and the second tool is an in-house developed substrate extraction tool.

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1 Introduction

1.1 Motivation

The amount of microelectronic devices such as microcontrollers, sensors used in automobiles has markedly increased in recent years. Due to the ever expanding amount of functionalities found in automobiles, efficient electrical power-management has become more important. This, among others, is a reason why so-called Smart Power ICs, "intelligent" power semiconductors, have taken on an increasingly important role in the automotive sector.

The down-conversion of the battery voltage to lower and more stable power supply is made possible by voltage regulators. The most efficient and therefore mostly adopted type of voltage regulators in Smart Power ICs are represented by switching circuits. A common type of the switched mode power supplies is the so-called DC/DC step-down converter, also known as buck-converter. In addition to the power components, Smart Power ICs also include analog and digital circuits which realize self-diagnostic and safety features [1].

In order to reduce costs and PCB space in automotive applications, multiple ICs are sometimes combined into a single chip, which then may contain power-management, sensor-interfaces and smart switches for components such as transceivers for bus-systems (e.g. CAN or LIN) [2, 3]. Often, it is desirable to combine all components of the Smart Power IC onto a single die which is called monolithic integration. This is opposed to connecting modules on separate dies using bond-wires in a so-called multi-die-package. Monolithic integration is made possible by means of very specialized and complex semiconductor technologies, that allow the fabrication of a wide range of different semiconductors on the same wafer. In the automotive sector, the most common type of semiconductor technologies used for monolithic integration are called BCD.

The high complexity, dense integration and large number of different semiconductor devices in BCD-technologies, however account for an increasing relevance of parasitic effects. Parasitic effects are caused by unwanted circuit elements, which in most cases are represented by small capacitors, resistors and inductors, resulting from the physical placement of devices (layout) of the IC. They can adversely affect the signal and power integrity within the IC, and thus lead to malfunctions.

In the integration of power switching blocks and RF blocks such as transceivers on the same die parasitic effects stand out in the form of substrate coupling issues. They are observed in the form of pronounced emissions caused by the switching of DC/DC step-down converters. It has been seen that, although operating at low frequencies such as of 300kHz - 2.2MHz [4, 5], very high harmonics near 100MHz of the buck-converters switching couple to nearby located transceiver pins [2]. Even these small "voltage ripples" may lead to the violation of EMC-standards. These emissions cannot be RC-filtered externally on the PCB because connecting an appropriate capacitance on the transceiver output would violate specifications of bus-systems used in the automotive sector [6]. Therefore, the most viable way in controlling these emissions is by means of a proper IC package design. While there exist plenty of well established tools for extracting parasitics of the metallization in the form of circuit elements, there is still no versatile tool for extracting the substrate with good accuracy and reasonable speed. Hence, to account for substrate during design, other techniques must be used.

1.2 The Goals of this Thesis

As mentioned in section 1.1, presently there are no commercially available extraction tools that can be used to obtain a parasitic circuit model that satisfy both our demands on accuracy

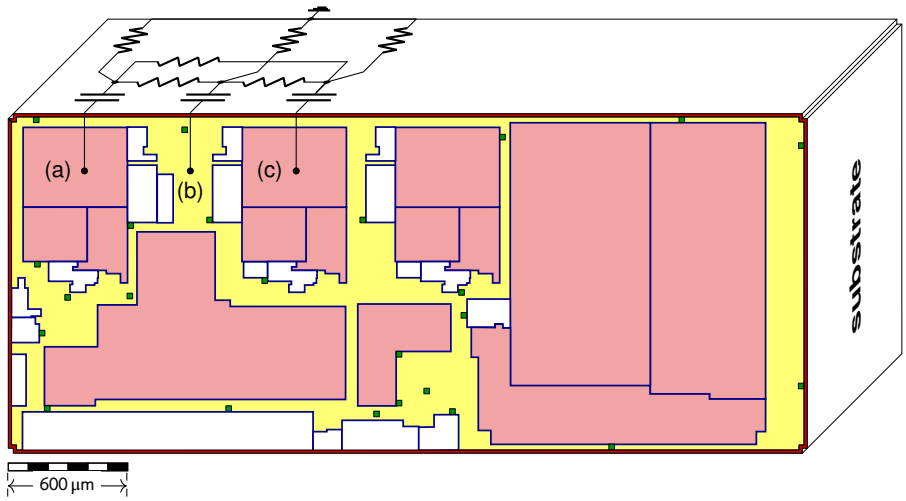


Figure 1.2.1: Illustration of our parasitc substrate circuit on a test chip from [3] (substrate height not to scale).

and simulation speed. One, particularly extreme approach, biased towards high accuracy but with strong deficits in simulation speed is to set up a full 3D FEM simulation of the substrate of a particular chip. In contrast to an automated parasitic extraction however, such an approach involves a considerable amount of manual work. Here, a designer would have to set up and manually optimize a 3D model and its mesh for compute performance. For the model to stay within the scope of what is nowadays feasible using high performance computing a significant amount of expertise in the utilization of FEM software is required, given the simulation is even posible at all.

To provide a better understanding of the substrate and at the same time help reduce the efforts in predicting substrate couplings, our first and main objective essentially comprises of constructing a simple parasitic substrate circuit containing only few components each representing a large structure. As illustrated in figure 1.2.1 such a simple model is useful when designing power switching and RF blocks on the same die to immediately obtain an approximate value for substrate couplings from region (a) to (c), in which emission sensitive devices may be placed. The distance between these devices represented by (b) can then be adjusted to an optimal value. We will show that for our parasitic model to be capable of accurately describing substrate couplings some of its resistors have to be frequency dependant. This is a result of a 2D FEM simulation of a very general substrate model, that is the basis on which the properties of our parasitic substrate circuit will be determined.

Our second goal is to use the parasitic substrate model we obtained from the 2D FEM simulations to evaluate some substrate extraction tools that are currently under development. The first tool we will test is the QRC substrate extraction solution by Cadence. As the accuracy of this tool is tied to a proper configuration, we will compare different configuration methods. As we will be described, the configuration methodology is very complex and an adequate configuration would rely on the knowledge of the partly undisclosed extraction technique it uses. The testing of QRC is aimed at obtaining a better understanding of its methodology.

The second tool is an in-house substrate extraction tool which will be examined regarding its accuracy.

1.3 Structure of this Thesis

The remainder of this thesis will be structured as follows: First we will provide some background information and theoretical concepts that are tied to the content of the practical part that follows. In the practical part we will outline our approach to achieving the goals stated in section 1.2 and present the results we obtained.

2 Theory

2.1 Parasitic Extraction

An essential part of the IC creation process is a circuit schematic that comprises of the circuit components through which the desired circuit in and output properties are realized. To verify if this circuit meets the wanted specifications, simulations of it are carried out using circuit simulators, such as SPICE. The input of circuit simulators is a so-called netlist which is a computer readable representation of an electrical circuit. Usually, a netlist lists the connections and attributes of each circuit component [7].

After a successful simulation of the schematic the next major step in the design flow comprises of the physical design of the IC. This mainly comprises of the layout which will have an impact on the ICs specifications. For instance, in the initial schematic the interconnect of components are represented by perfect electrical conductors (PEC), however wires have limited conductivity, show inductive behaviour and are capacitively coupled between each other and to the underlying substrate. Depending on the physical placement of the devices, these so-called parasitic effects may lead to functional failures and violations of EMC standards. EDA (electronic design automatization) tools, usually used by designers for the IC creation, often include parasitic extraction solutions that lump these effects into additional parasitic devices (capacitors, resistors and inductors), augmenting the original netlist of the schematic.

The inclusion of parasitic elements is known to drastically increase the run time of simulators which is why trade-offs for accuracy are made to increase computational performance. Essentially, these extraction tools BEM or FEM discretize Maxwell's equations in the relevant domain and use additional methods to further spasify the resulting matrices of the underlying equations. Such a method could, for instance, be represented by the so-called fast mulipole BEM method which reduces the number of computing operations quadratically from a conventional BEM discretization. The exact methodologies however are proprietary knowledge of the extraction tool vendors [8].

Top-level parasitic extraction, parasitc effects caused mostly by the metallization, is always necessary, whereas parasitic effects caused by substrate couplings are in many cases considered to be less relevant. However, the monolithic integration of power switching blocks and RF blocks brings substrate coupling issues to the forefront [3]. Substrate extraction is therefore required which refers to methods which build a circuit model of the substrate that can be merged with the top-level netlist.

After the extraction of parasites, the physical design verification can then be carried out by simulating the complete netlist which includes all parasitic components, and is successful if the results still meet the desired specifications of the circuit.

2.2 The considered BCD-Technology

Especially in semiconductor engineering, it is important to strongly optimize a product regarding cost and performance. An important part of this the development of an appropriate semiconductor technology. The term semiconductor technology refers to the process steps which are the means of fabricating a semiconductor. In theory, the highest level of optimization regarding performance would be reached if the technology an IC uses is specifically tailored for the functionality of that specific chip. However, in most cases, this is economically far from sensible as the development and series production of a wafer technology is tied to an enormous financial investment. As a result, semiconductor manufacturers possess a range of technologies, each of which is tailored to a particular product group. A product group can for instance be represented by a portfolio of ICs that contain only digital com-

ponents. Over the years each manufacturer has optimised each of these technologies to their product portfolio and their details are often a strongly protected intellectual property of the company.

Driven by a competitive market and higher demands for safety and functionality, power electronics nowadays, calls for a variety of technologies of which some of the most important types are *Bipolar*, *CMOS* and *DMOS*. *Bipolar* is the technology used to make precise analog devices, *CMOS* (Complementary Metal Oxide Semiconductor) is used for digital design and *DMOS* (Double Diffused Metal Oxide Semiconductor) for power and high-voltage elements. Especially in the automotive sector, the smart power ICs, mentioned in section 1.1, rely on these technologies for the implementation of their wide range of functionalities, including self diagnosis functions (overcurrent detection, overtemperature detection, reverse current protection, etc.) and control systems (slew rate control, automatic PWM/PFM-mode selection, feedback loop, standby mode, etc.). As opposed to former times, a monolithic integration of the devices that make up a Smart Power IC today, represents, despite its high costs, a commercially sensible approach. *BCD* (Bipolar-CMOS-DMOS) is the semiconductor technology that integrates fabrications processes of Bipolar, CMOS and DMOS, such that devices of each technology can be placed on the same die [2].

In this section we briefly discuss the BCD technology we analyze. Figure 2.2.1 shows a cross sectional view of a die in which some important devices in this technology are depicted. The discussion will be centered around the purposes of each of these devices, their fabrication methods, however, are beyond the scope of this work.

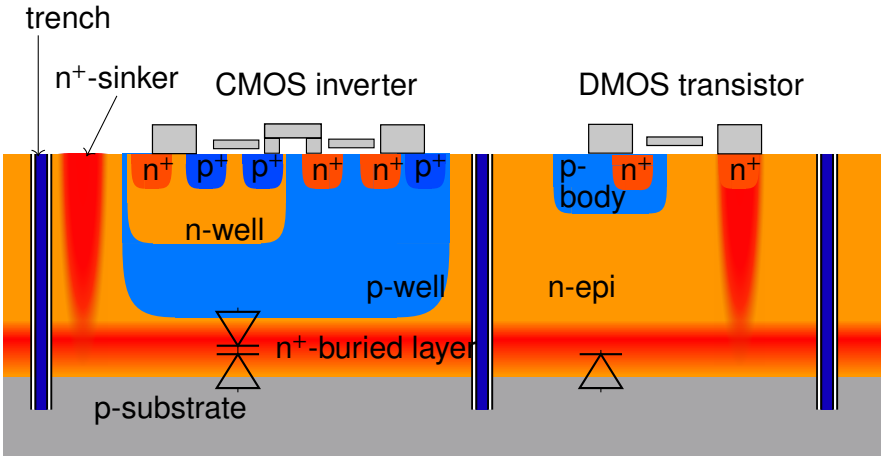


Figure 2.2.1: Cross sectional view of the considered BCD-technology. As an example, a CMOS inverter residing inside the p-logic region (left) and a power DMOS transistor (right) is depicted.

The starting point of the semiconductor processing is a silicon wafer with a homogeneous and controlled doping. In the technology we consider, this wafer is lightly doped with acceptor (p^-) atoms, and therefore, is called a p-type wafer. A wafer doped with donor atoms (n^-), on the other hand, is termed an n-type wafer [9]. After grinding, a large part of this initial wafer remains present, which is also called the *wafer-level-substrate*[1] ($\sim$ 200µm in thickness). The subsequent processing steps only modify the top of the substrate ($\sim$ 20µm), whereas the rest remains unaffected.

[1]We will call this layer of the wafer just *substrate* from here on wards. It should be noted that in some related literature the term substrate includes the epi-layer which is added in a later process step.

Above the substrate a new n-type layer is grown epitaxially, hence it is called the *n-epitaxial layer* (epi-layer) of which the bottom most part is heavily doped (n^+) during its growing process. This leaves the wafer with a highly conductive layer located just above the substrate and beneath the remainder of the epi-layer. It is termed the *n^+-buried layer* the purpose of which will be discussed later.

After the n-epi-layer was grown, so-called *p-wells* are implanted in some regions of the chip. Implanting impurities of a different kind (p or n) is a very common process step, and, essentially, locally converts n-doped silicon to p-doped silicon or vice versa [10]. These special p-wells serve as a pseudo-substrate enabling therein the inclusion of a CMOS-technology designed for a p-type substrate.

In these regions, two diodes are formed through the n^+-buried layer (see figure 2.2.1, left) – the first one with the substrate below, and the second with the p-well above. If the n^+-buried layer is biased to a suitable voltage (ca. -60V to +0.6V), causing the depletion regions of both diodes to increase (reverse biased), the n^+-buried layer almost perfectly isolates the substrate from the epi-layer galvanically (pn-junction isolation). To set the voltage of the n^+-burried layer, it is required to contact it electrically, which is achieved by so-called *n^+-sinkers*.

An *n^+-sinker* is a heavily doped (n^+), pillar shaped region reaching from the chip-surface down to the n^+-buried layer. This sinker is then electrically connected to the metal interconnect layers by means of electrical vias.

A *deep trench*[2] separates two different groups of circuits and removes lateral parasitic bipolar transistors between them. It is composed of some poly-silicon between two isolating oxide layers, and reaches down to the top of the substrate cutting the n^+-buried layer into fragments enabling each fragment to be connected to a different potential. Thus, some fragments of the n^+-buried layer are used as a functional terminal of a power device such as the drain (or source) of a DMOS. The conductor inside the trenches must be doped silicon to match the thermal expansion coefficient of the surrounding silicon, and allows for an electrical connection of the substrate from above, which in our case, as it is usually, leads to "ground", ensuring the junction isolation to be only dependant on the potential of the n^+-buried layer [11].

2.3 Electric Conduction Constitutive Laws

The electric field within any material is described by Maxwell's equations in matter. Assuming that inductive effects are negligibly small, implying $\nabla \times \vec{E} \approx 0$, then the electric field is tied only to its scalar potential ϕ:

$$\vec{E} = -\nabla\phi \tag{2.3.1}$$

In order to find a differential equation that is connected to ϕ we will look at the following of Maxwell's equations in matter:

$$\nabla \times \vec{H} = \vec{J_f} + \sigma\vec{E} + \frac{\partial \vec{D}}{\partial t}, \tag{2.3.2}$$

where

$$H = \frac{\vec{B}}{\mu_0} + \vec{M}(\vec{B}),\ D = \epsilon_0\vec{E} + \vec{P}(\vec{E})$$

Here, $\vec{M}(\vec{B})$ denotes the magnetization and $\vec{P}(\vec{E})$ the polarization density of the material.

[2] In the following deep trenches are refered to as *trenches*

In applying the divergence operator on equation 2.3.2 and using the identity[3] $\nabla \cdot \nabla \times \vec{A} = 0$ we obtain:

$$0 = \nabla \cdot \vec{J}_f + \nabla \cdot (\sigma \vec{E}) + \nabla \cdot \frac{\partial \vec{D}}{\partial t} \tag{2.3.3}$$

For material that is both linear and isotropic we can write $\vec{D} = \epsilon \vec{E}$, where $\epsilon = \epsilon_0 \epsilon_r$, and assuming our problem does not involve any free currents we are left with equation:

$$0 = \nabla \cdot (\sigma \vec{E}) + \nabla \cdot \frac{\partial \epsilon \vec{E}}{\partial t} \tag{2.3.4}$$

For an AC-conduction problem we can eliminate the time derivative by using an ansatz of the form $A \exp\{i\omega t\}$, where A represents a complex valued amplitude. This yields:

$$0 = \nabla \cdot (\sigma \vec{E}) + \nabla \cdot (i\omega \epsilon \vec{E}) \tag{2.3.5}$$

Substituting equation 2.3.1 and rearranging gives:

$$0 = \nabla \cdot ((\sigma + i\omega\epsilon)\nabla\phi) \tag{2.3.6}$$

Hence, solving for the electrical field while neglecting inductive effects for any material of electric conductivity σ and dielectric permittivity ϵ_r boils down to solving equation 2.3.6. This equation can be classified as a linerar, homogenious, partial differential equation of second order. In the special case of σ and ϵ being not dependant on spacial position equation 2.3.6 simplifies to Laplace's equation. There are only few cases for which an analytical solution for 2.3.6 can be found, most of which are highly symmetric. For all other cases, solving equation 2.3.6 requires numerical methods such as *Finite Element Method* (FEM) or *Boundary Element Method* (BEM) [12].

2.4 Network Theory

2.4.1 Y-parameters and Z-parameters

In electrical engineering applications where electric and magnetic fields within an electrical network are of less interest than the networks behaviour at specific points, it is useful to find a representation of this network only relating the quantities of interest such as current or voltage at these specific points to each other. Such a representation of a network is realized in form of a so-called network parameter matrix. We will see in the following that it allows us to obtain the small signal response of the network for an AC-voltage or AC-current excitation at any chosen points. To obtain the network parameter matrix of a network, the points, at which the currents and voltages are of interest, have to represent a *port* [13, 14].

A *port* of an electrical network is defined as a pair of terminals that satisfy the so-called port condition: The port condition requires the two terminals to have equal but opposite current flowing through them. We will constrain our discussion to networks that have ports of which the second terminal is internally shorted and is common to all ports. Such a network is illustrated in figure 2.4.1.

The network parameter matrix of an electrical network with N ports is given by a (complex-valued) frequency-dependant $(N \times N)$-matrix. There exist multiple matrix conventions describing an N-port network, however we will limit our discussion to the so-called impedance matrix and admittance matrix.

[3] $\vec{A}$ is an arbitrary vector field.

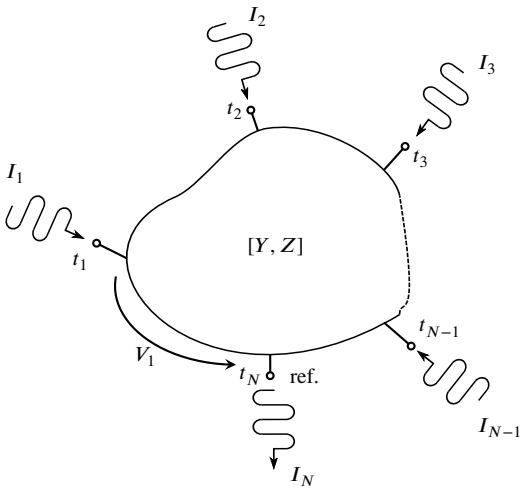


Figure 2.4.1: An arbitrary N-port network with common reference terminal t_N.

We define the voltage of port n to be the voltage that can be measured between terminals n and N if a current source is connected between these terminals. We define the current I_n as the current entering terminal n, which is equal to that leaving terminal N, if a voltage source is connected between n and N.

The impedance matrix, also refered to as *Z-parameter matrix* is defined by equation 2.4.2. Hence, the entries of Z are given by:

$$Z_{i,j} = \left.\frac{U_i}{I_j}\right|_{I_k=0 \text{ for } k\neq j} \tag{2.4.1}$$

In words, each matrix element is calculated under open circuit conditions, This means, the $Z_{i,j}$-element of the Z-parameter-matrix represents the impedance (Z) which can be measured at port i while port j is replaced by a current source and all the other ports are left unconnected, equalling each to an Impedance of ∞ ("open") and thus zero current flows through them.

$$\begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ U_N \end{bmatrix} = \begin{bmatrix} Z_{1,1} & Z_{1,2} & \cdots & Z_{1,N} \\ Z_{2,1} & \ddots & & \\ \vdots & & & \\ Z_{1,1} & & & Z_{N,N} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} \tag{2.4.2}$$

Similarly, the admittance matrix also known as *Y-parameter matrix* is defined by equation 2.4.3. Hence, the entries of Y are given by:

$$Y_{i,j} = \left.\frac{I_i}{U_j}\right|_{U_k=0 \text{ for } k\neq j}$$

In words, the matrix elements of Y are calculated under short circuit conditions. This means, the $Y_{i,j}$-element of the Y-parameter-matrix represents the conductance (1/Z=Y) which can be measured at port i while port j is replaced by a voltage source and all the other ports are shorted, equalling each to an Impedance of 0 ("short") and thus the voltage over them is zero.

By comparing 2.4.2 and 2.4.3 we can see that Z and Y are inverses of each other:

$$Y^{-1} = Z$$

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{1,1} & Y_{1,2} & \cdots & Y_{1,N} \\ Y_{2,1} & \ddots & & \\ \vdots & & & \\ Y_{1,1} & & & Y_{N,N} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ U_N \end{bmatrix} \tag{2.4.3}$$

2.4.2 Reciprocal networks and their equivalent circuits

A network is termed *reciprocal* if its network parameter-matrix is equal to its transpose (e.g. $Y = Y^T$). Physically, this means that the current, measured at port i, while a voltage is applied at port j, is equal to the current that would be measured at port j if the same voltage was applied at port i. This applies to networks of linear passive components, that is, they may only contain Rs, Cs, and Ls (including inductive couplings K).

Given arbitrary reciprocal n-port network parameters there are two important equivalent circuit representations consisting of frequency dependant two-terminal impedances only. They are called the T-equivalent, derived from Z-parameters and the Π-equivalent, derived from Y-parameters [14]. We will discuss the Π-equivalent in the following.

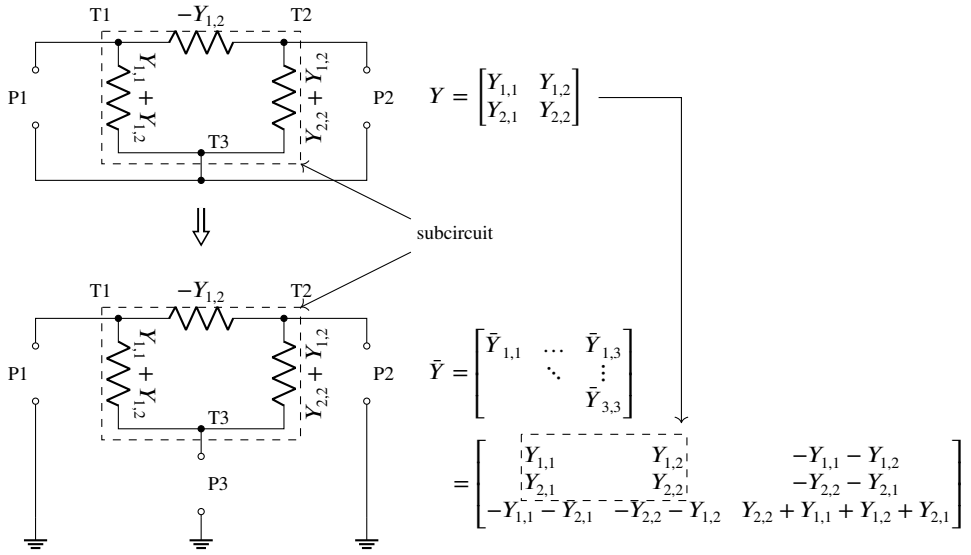


Figure 2.4.2: 2-port (top) to 3-port (bottom) transformation of an arbitrary Π-equivalent.

Let us now consider a reciprocal 2-port network, the ports of which have a common reference. The impedances of its Π-equivalent can be obtained using the entries of its Y-parameter matrix, as illustrated in figure 2.4.2 (top).

We will now examine a transformation which changes the port reference from the common terminal T3 to ground, and hereby add port P3, as shown in figure 2.4.2 (bottom). The Y-parameter matrix $\bar{Y}$ of our obtained network with an external ground as reference contains Y as upper left sub-matrix. The additional row and column corresponding to port P3 can be computed on the basis that rows and columns of $\bar{Y}$ add to zero. This is due to the fact that for the excitation of any port(s) now the current entering the subcircuit has to be equal to the current leaving the subcircuit.

As we can see in figure 2.4.2 the subcircuit remains the same, however the two-terminal impedances are now equal to the negative off-diagonals of $\bar{Y}$.

Note that the network with external ground as reference has a valid Y-parameter representation, however, according to their definition (section 2.4.1), the entries of its Z-parameter matrix would equal ∞.

The above described transformation can be applied to any n-port Π-equivalent, which are essentially reciprocal networks with ports that all share a single common reference.

This transformation can also be applied inversely, which amounts to deleting some row and column j. By applying this transformation and then applying its inverse for a different reference terminal, we can change a common terminal from one terminal to another.

2.4.3 Y-delta transform

In section 2.4.2 we have mentioned that any reciprocal network can be represented in a Π-equivalent or a T-equivalent, the impedances of which can be computed using the networks Y and Z-paramters respectively. Let us consider an arbitrary 2-port for which the Π and T-equivalent is illustrated in figure 2.4.3. The subcircuit highlighted by dashed lines in the Π-equivalent can be regarded as a Δ-circuit and that in the T-equivalent as a Y-circuit. Since both networks have the same properties, these subcircuits are equivalent transforms of each other. Using the Y and Z-parameters of this network we will in the following show how we can obtain the impedance values of the Δ-circuit in terms of that in the Y-circuit.

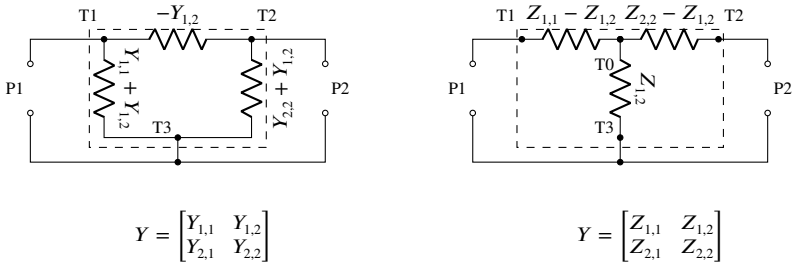


Figure 2.4.3: Π and T-network. The highlighted subcircuits in each network can be regarded as a Δ and a Y-circuit respectively.

We define:

$$\text{G1M} = -Y_{1,2},\ \text{G2M} = Y_{1,1} + Y_{1,2},\ \text{G3M} = Y_{2,2} + Y_{1,2}$$

and

$$\text{R1} = Z_{1,2},\ \text{R2} = Z_{1,1} - Z_{1,2},\ \text{R3} = Z_{2,2} - Z_{1,2}$$

Since the inverse of Z is equal to Y, the Y-parameter matrix of our 2-port can be written using the entries of its Z-parameter matrix:

$$Y = Z^{-1} = \frac{1}{Z_{1,1}Z_{2,2} - Z_{2,1}Z_{1,2}} \begin{bmatrix} Z_{2,2} & -Z_{1,2} \\ -Z_{2,1} & Z_{1,1} \end{bmatrix} \tag{2.4.4}$$

Let us now compute G1M which is equal to $-Y_{1,2}$ using the expression in 2.4.4:

$$\text{G1M} = Y_{1,2} = \frac{Z_{1,2}}{Z_{1,1}Z_{2,2} - Z_{2,1}Z_{1,2}} \tag{2.4.5}$$

The nominator in 2.4.5 is equal to R1. In terms of R1, R2, and R3 it can be shown that the denominator is given by:

$$Z_{1,1}Z_{2,2} - Z_{2,1}Z_{1,2} = \underbrace{\text{R1} \cdot \text{R2} + \text{R1} \cdot \text{R3} + \text{R2} \cdot \text{R3}}_{RR} \tag{2.4.6}$$

By proceeding analogously for G2M and G3M we will get:

$$\mathrm{G1M} = \frac{\mathrm{R1}}{RR},\ \mathrm{G2M} = \frac{\mathrm{R3}}{RR},\ \mathrm{G3M} = \frac{\mathrm{R2}}{RR} \tag{2.4.7}$$

A slighlty simpler expression can be obtained using the conductances $\mathrm{G1} = \frac{1}{\mathrm{R1}}$, $\mathrm{G2} = \frac{1}{\mathrm{R2}}$ and $\mathrm{G3} = \frac{1}{\mathrm{R3}}$ by multiplying nominator and denominator of the above equations by:

$$\frac{1}{\mathrm{R1} \cdot \mathrm{R2} \cdot \mathrm{R3}}$$

This yields:

$$\mathrm{G1M} = \frac{\mathrm{G2} \cdot \mathrm{G3}}{GG},\ \mathrm{G2M} = \frac{\mathrm{G1} \cdot \mathrm{G2}}{GG},\ \mathrm{G3M} = \frac{\mathrm{G1} \cdot \mathrm{G3}}{GG} \tag{2.4.8}$$

where

$$GG = \mathrm{G1} + \mathrm{G2} + \mathrm{G3}$$

Expressions for the impedances of the Δ-circuit in terms of the Y-circuit impedances can be obtained by substituting and rearranging equations in 2.4.7 or 2.4.8.

2.4.4 Interconnection of n-port networks

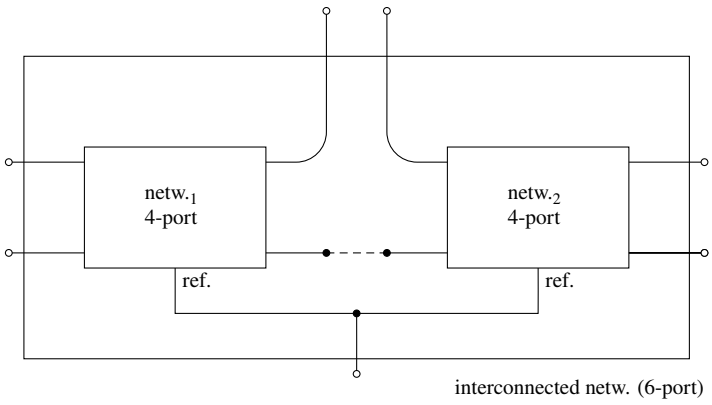


Figure 2.4.4: Interconnection of two arbitrary 4-ports forming a 6-port network.

An interconnection of networks is accomplished by connecting a port of one network to a port of another, resulting in a new network that can be described by its own network parameters. In the case of measured network parameters, the removal of effects (e.g. contact resistance) caused by components which could not be removed by a calibration is achieved through such an interconnection. This procedure is called de-embedding, and involves the cascading of the inverse of a network containing the unwanted components and the measured network, yielding the network that was intended to be measured. If the internal circuit elements of a network are known, or a least the ones directly connecting to the networks ports a similar procedure can be carried out as a means of subdividing the network. In this case, the cascading of the inverse network parameters of circuit devices will yield a smaller "portion" of the initial network. Consequently, the subsequent cascading of the same non-inverse network parameters will result in the original network.

In this section, we will present a way of obtaining the Y-parameter matrix of an $(n+m-2)$-port network, which is defined by connecting an n with an m-port. This is illustrated in figure 2.4.4 for two 4-ports. Our approach will be analogous to the one presented in [15].

We proceed in two steps: First we put together the m-port A and the m-port to form an $(n+m)$-port C (see figure 2.4.5 top). interconnected n-ports. The Y-parameter matrix of C is obtained by simply appending Y_B to Y_A diagonally.

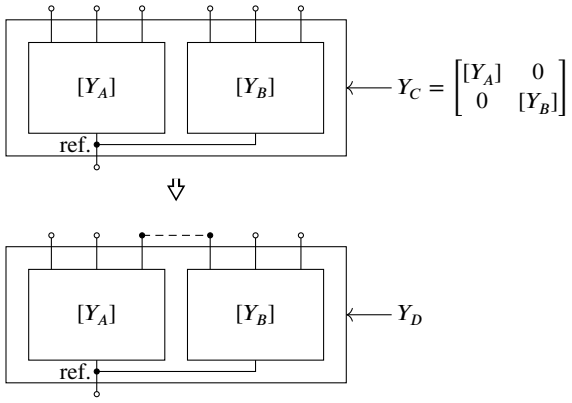


Figure 2.4.5: Eliminating two ports of a network by connecting the with each other.

Then we eliminate two ports from C, by connecting two ports of C each of which formerly belonged to A and B respectively as illustrated in figure 2.4.5 (bottom), to form network D an $(n+m-2)$-port.

Let us assume these ports have indices k and l in Y_C, defined by equation 2.4.9:

$$\begin{bmatrix} I_1 \\ \vdots \\ I_k \\ \vdots \\ I_l \\ \vdots \\ I_N \end{bmatrix} = \underbrace{\begin{bmatrix} Y_{1,1} & & & \cdots & & & Y_{1,N} \\ & \ddots & & & & & \\ & & Y_{k,k} & \cdots & Y_{k,l} & & \\ \vdots & & \vdots & & \vdots & & \vdots \\ & & Y_{l,k} & \cdots & Y_{l,l} & & \\ & & & & & \ddots & \\ Y_{N,1} & & & \cdots & & & Y_{N,N} \end{bmatrix}}_{Y_C} \begin{bmatrix} U_1 \\ \vdots \\ U_k \\ \vdots \\ U_l \\ \vdots \\ U_N \end{bmatrix} \tag{2.4.9}$$

From Y_C (from now on $Y_C = Y$, to avoid excessive indexing) we now would like to obtain Y_D. Our starting point are the following conditions which equal to a connection of the ports k and l:

$$-I_k = I_l \tag{2.4.10}$$

$$U_k = U_l \tag{2.4.11}$$

Inserting 2.4.10 in 2.4.9 yields:

$$-\sum_{i}^{n+m} Y_{k,i} U_i = \sum_{i}^{n+m} Y_{l,i} U_i \tag{2.4.12}$$

By rearranging 2.4.12 and substituting 2.4.11 we obtain:

$$U_k = U_l = -\frac{1}{Y_{k,k} + Y_{k,l} + Y_{l,k} + Y_{l,l}} \sum_{i \neq i,k}^{n+m} (Y_{l,i} + Y_{k,i}) U_i \tag{2.4.13}$$

Substituting 2.4.13 into 2.4.9 yields the new Y-parameter matrix Y_D of dimension $n+m-2 \times n+m-2$, of which the matrix-elements are computed by:

$$Y_{D,i,j} = Y_{i',j'} - \frac{1}{Y_{k,k} + Y_{k,l} + Y_{l,k} + Y_{l,l}}(Y_{l,j'} + Y_{k,j'})(Y_{i',l} + Y_{i',k}) \tag{2.4.14}$$

where $i', j' \in [1, n+m] \setminus \{k, l\}$ and $i, j \in [1, n+m-2]$

To compute an interconnection of multiple n-ports the above procedure must be applied iteratively.

3 Computer Experiments

3.1 FEM Simulation using Ansys Maxwell 2D

3.1.1 Construction of a simplified 2D model used to obtain general parameters of substrate couplings

Our goal, as mentioned in section 1.2, is to construct a discrete parasitic substrate circuit describing substrate couplings between to adjacent devices on a die. To obtain the properties of its circuit components we will carry out FEM simulations of a substrate model. In our approach to find an appropriate FEM simulation model that can adequately describe our problem, we assume that the distance d between two particular devices, as illustrated in figure 3.1.1, and the height of the substrate are much more crucial parameters than the lateral extent of the devices. We will therefore avoid a full 3D FEM simulation, by reducing the dimensions to 2D, requiring a significantly lower amount of time and computational resources, but as a consequence, neglect fringe fields that may occur near lateral boundaries. Furthermore, we will neglect any inductive behaviour within the considered domains, which however would represent an equally reasonable approximation in a 3D simulation.

Figure 3.1.1 (A-A) shows the cross sectional view of two adjacent devices on an exemplary die. It comprises of an arbitrary device including the epi-layer (a), the buried layer (b) and the substrate (c). For our parasitic substrate circuit we would like to approximate the pn-junctions formed by the buried layer fractions each to a single parallel plate capacitor. The substrate itself will be represented by a very sparse resistor network. This topology, in the least, ensures an accurate behaviour of the domain our parasitic substrate circuit represents in the frequency limits $f \to 0$ and $f \to \infty$. Since the capacitors can easily be calculated, this means from our FEM simulation we only need to be able to obtain the values for the resistors.

By cutting off everything that lies above section line s_1, our model would embody the substrate alone, and a simulation of it would yield a frequency-*in*dependant network of resistors, given that we prescribe a voltage field at s_1 independant of f. We would then have to make assumptions about the field at s_1, however at this point it is unclear what this should be. We will therefore have to expand this model to obtain boundaries of which we know the conditions, or at least can make reasonable approximations of. It has been observed by our group that it is often a good approximation to regard the highly conductive buried layer as a perfect electrical conductor. Therefore, cutting at s_2, and applying a constant voltage boundary condition is reasonable. Since now the distributed capacitance of the pn-junctions are part of our FEM simulation model, a carefully designed parameter extraction procedure is required (see section 3.1.3) to separate them from the bare substrate resistor network from which we would like to obtain the values of our parasitic substrate circuit.

In using single capacitors for each buried layer fraction, the resistor network of our parasitic substrate circuit is completely independant of the value of these capacitors. We can now also attempt to make the resistors in our circuit that are decisive for the coupling between the buried layer fraction only dependant on the distance d and the height h of the substrate. Since the bulk of the coupling current flows close to the edges, as we will be discussed in section 3.1.4, this is achieved by setting the length l of the outer fractions of the buried layer to a large value approximating the limit $l \to \infty$. We will simulate our FEM model for different values of d to examine our models dependency on it.

Ultimately, if it is possible for our simple model to describe substrate couplings, then a circuit designer can, just like us, approximate the buried layers in their layout to a single capacitance and use the resistor data we provide for this parasitic substrate circuit to predict an approximate value for noise couplings. This, however, is only possible if we can determine the values of the resistors, at least for certain frequency intervals, such that our parasitic model

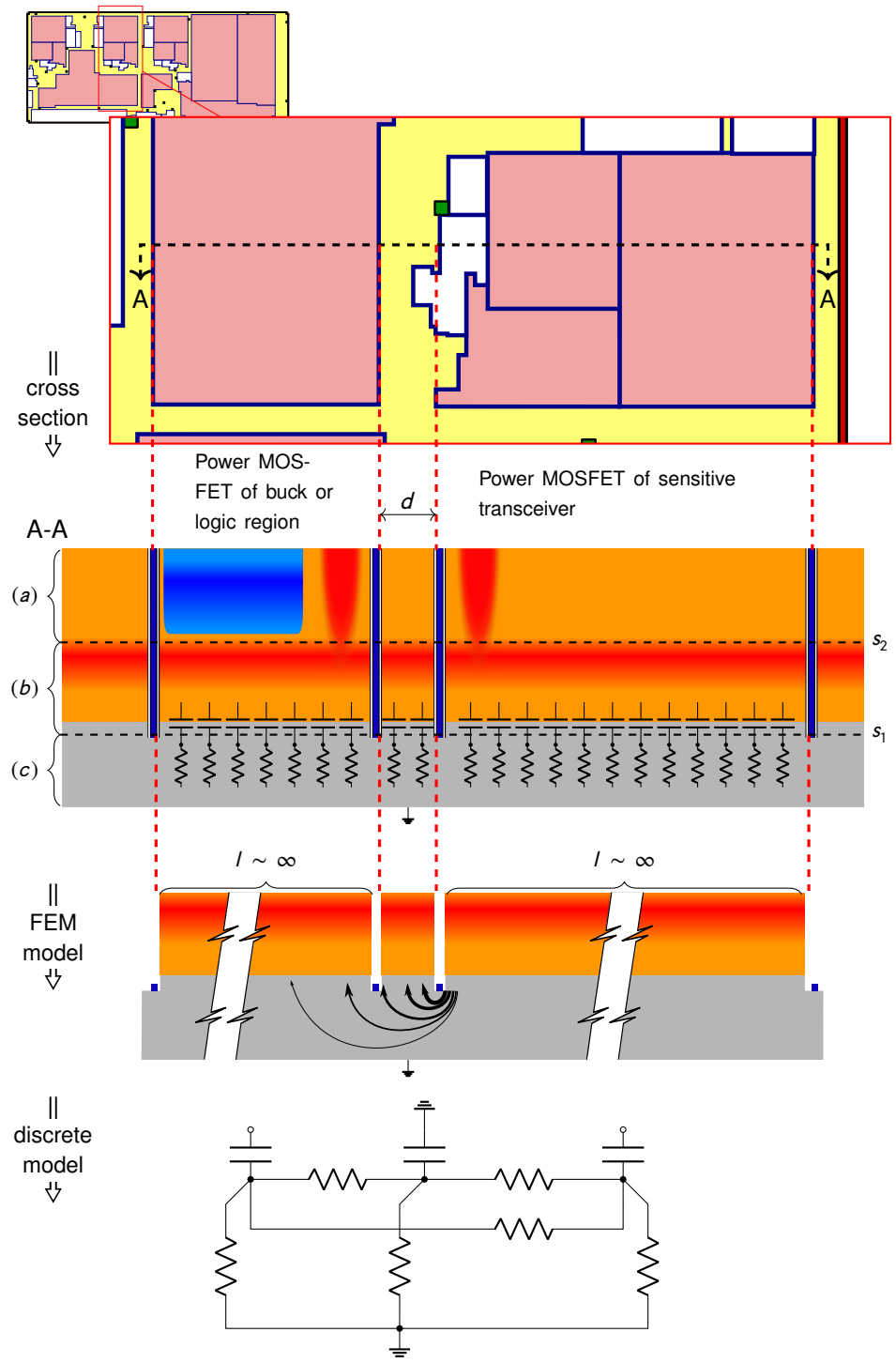


Figure 3.1.1: 2D abstraction of a substrate coupling issue from which an appropriate FEM simulation model can be extracted that can be further discretized to a low-dimensional parasitic substrate circuit. Substrate and epi-layer height are not to scale.

is in reasonable agreement with our FEM simulation. Here, it should be noted that the backside of our simulation is always perfectly connected to some potential (e.g. "ground"). In ICs with grounded backside this is an excellent approximation, whereas in ICs with unconnected backside large deviations must be expected.

3.1.2 Obtaining the full Y-parameter matrix using Ansys Maxwell 2D

The complete model we implement in Ansys Maxwell 2D is depicted in figure 3.1.2. Since we will approximate the buried layer to a perfect electrical conductor, an implementation of a dopant profile is not required. The capacitance of the pn-junction between the buried layer and the substrate is modelled using a dielectric material (pn-junction isolation; see section 2.2). Its height h_{pn} and dielectric permittivity ϵ_r are chosen such that the resulting capacitance per unit length matches the one of the pn-junction at 0V bias voltage. In section 3.1.6 we will illustrate how our data can be converted to represent a case where the buried layer capacitance differs from the one we use. The material we choose for the substrate in our simulation will have the nominal conductivity of the substrate in our considered technology.

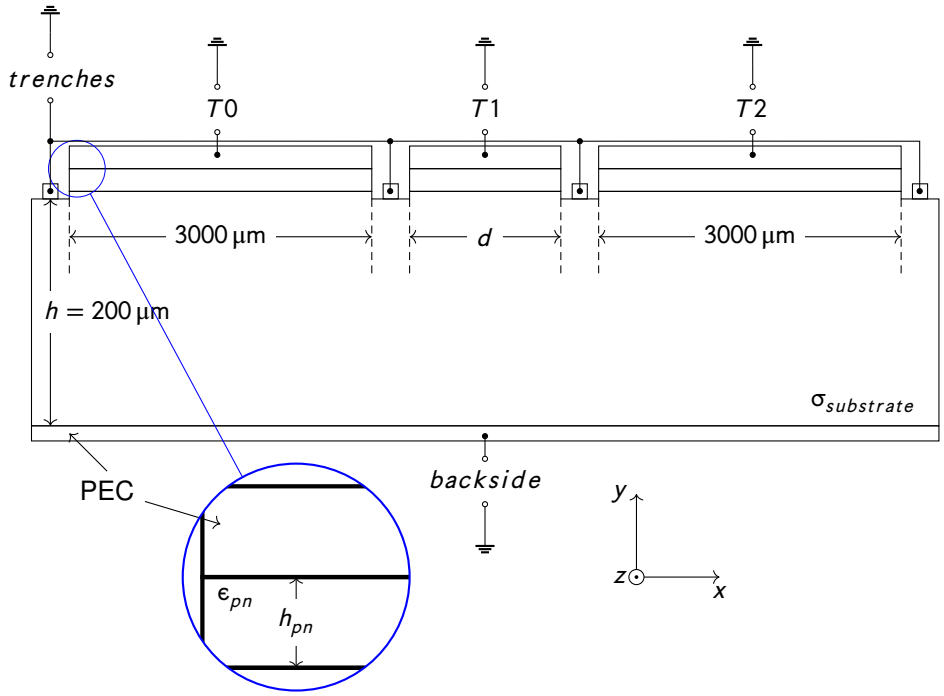


Figure 3.1.2: 2D FEM model implementation for the simulation of Y-parameters

The length of the buried layer fractions represented by $T0$ and $T2$ will be 3000µm (∞-limit). The height of the substrate h will be 200µm. In section 3.1.6 we will present a way to convert the data we obtained to different substrate heights. The distance d, which is the length of the buried layer represented by $T1$, is an important parameter and will be varied.

For each distance d, we will simulate the Y-parameter matrix of our model. The terminals in this Y-parameter representation are $T0$, $T1$, $T2$, *backside* and *trenches*, as shown in figure 3.1.2. We do not distinguish between different trenches, and they are thus shorted and connected to the same terminal (see figure 3.1.2).

Since the Y-parameter representation of our model can be regarded as an exhaustive small signal characterization of this model, we can obtain the response of the network for any excitation (see section 2.4.1). Therefore, no further characterization besides Y-parameters is required. As our model does not contain any active elements (e.g. transistors), the Y-parameter matrix we obtain from the simulation is reciprocal and can be represented as a Π-equivalent circuit (see section 2.4.2). We bring the Y-parameters into a form, as illustrated

$$\begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ U_4 \\ U_5 \end{bmatrix} = \underbrace{\begin{bmatrix} Y_{1,1} & Y_{1,2} & Y_{1,3} & Y_{1,4} & Y_{1,5} \\ & & Y_{2,3} & Y_{2,4} & Y_{2,5} \\ \vdots & & \ddots & Y_{3,4} & Y_{3,5} \\ & & & & Y_{4,5} \\ Y_{5,1} & & \cdots & & Y_{5,5} \end{bmatrix}}_{Y_F = Y_F^T} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \begin{matrix} T0 \\ T1 \\ T2 \\ trenches \\ backside \end{matrix}$$

Figure 3.1.3: Y-parameter representation of the simulated model depicted in figure 3.1.2.

in figure 3.1.3, where each off-diagonal element can be mapped to the impedance between two terminals of the Π-equivalent (see section 2.4.2). This is indicated by the port symbols in figure 3.1.2. All of our calculations that follow are based on this Y-parameter matrix representation. Note that the entries of this Y-parameter matrix are complex-valued.

3.1.3 Using the simulated Y-parameters to determine the resistor values of our parasitic substrate model

As described in section 3.1.2, our FEM simulation model does not embody the substrate alone but includes the buried layer. Hence, the impedances of the Π-equivalent circuit of our obtained Y-parameters also account for the capacitive effects caused by the pn-junctions. As mentioned in section 3.1.1, we would like to approximate the pn-junctions each to a single parallel plate capacitor. This means, we have to find out whether the frequency dependant impedances of the Π-equivalent of our Y-parameters can be represented by the discrete components illustrated in figure 3.1.4.

In this section we outline our approach for obtaining the bare substrate consisting of the resistors shown in figure 3.1.4, from the Y-parameters Y_F of the FEM-simulation. In our approach to determine the resistor values we will, for now, have to allow these resistors to both be complex-valued and frequency dependant. In section 3.1.4 we will then examine the extent to which these values deviate from a real resistor. The phase and frequency dependance will have a notable impact on the degree to which our data can be used. That is, if the resistors are not dependant on frequency, or at least piece wise constant in particular frequency domains, simple ideal resistors can be used in SPICE-circuit simulation. In the case of an arbitrary frequency dependance our data could still be used by advanced methods like vector-fitting [16]. Vector-fitting reproduces a frequency dependant impedance by fitting rational functions, and converting the fit parameters into a complicated equivalent circuit. However, it is well known that vector-fitting often leads to unexpected and incorrect results, requires manual tuning and can render transient simulation unstable.

The components of our parasitic substrate circuit of which we already know the values of are represented by the capacitors. Their values are computed by:

$$\mathrm{C0} = \mathrm{C2} = \epsilon_0 \epsilon_{pn} \frac{l}{h_{pn}} \left[\frac{\mathrm{F}}{\mu\mathrm{m}}\right]$$

$$\mathrm{C1} = \epsilon_0 \epsilon_{pn} \frac{d}{h_{pn}} \left[\frac{\mathrm{F}}{\mu\mathrm{m}}\right]$$

Now, to find out if the Π-equivalent of our FEM Y-parameters can be represented in the topology shown in 3.1.4, consider the equivalence transform of Y_F shown in figure 3.1.5. Here, the negative capacitors $-\mathrm{C0}$, $-\mathrm{C1}$ and $-\mathrm{C2}$ have been connected to the terminals $T0$,

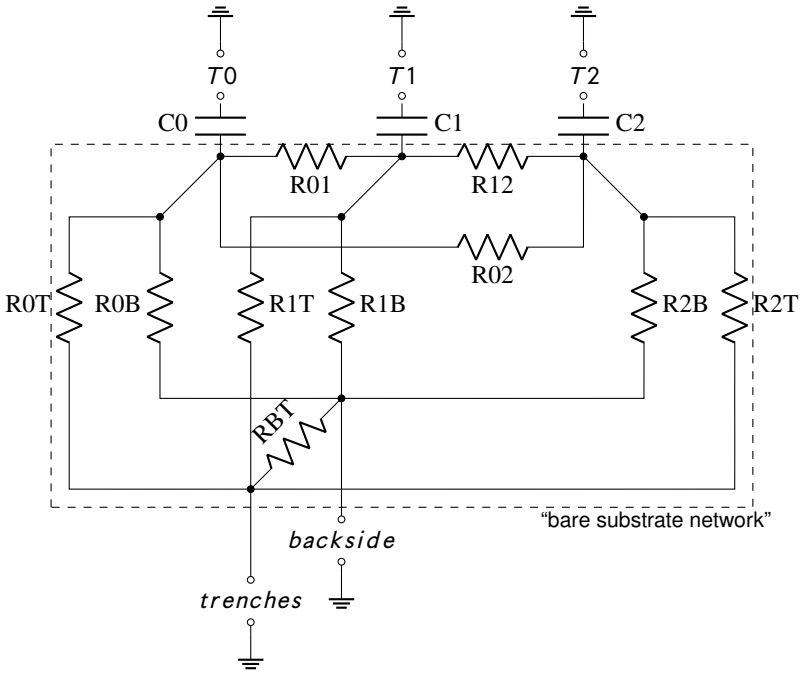


Figure 3.1.4: All components of the parasitic substrate circuit. Each pn-junction is represented by a single capacitor, and the resistors each represent a 2-terminal impedance in the bare substrate network.

$T1$ and $T2$ respectively, which results in matrix Y_B. By connecting the same only positive capacitors to Y_B we get Y_M which trivially equals Y_F. This in turn means that Y_B hast to represent the bare substrate network. Thus, its Π-equivalent must contain only real resistors, or such that can be regarded as within a considered frequency range, given our parasitic substrate model can be realized. Verifying this, boils down to simply examining the off-diagonals of Y_B which each corresponds to an impedance in its Π-equivalent and therefore to one of the resistors shown in figure 3.1.4.

The connecting of the negative capacitors to obtain Y_B can be carried out by representing each capacitors in their appropriate network parameter matrix and using the formulae provided in section 2.4.4.

Note that it is important that our parallel plate capacitor approximation is justifiable. This means their capacitance has to reasonably match that of the distributed capacitors of the pn-junctions. Otherwise Y_B would still contain relics of the negative pn-capacitance of our model, and the results we obtain from it cannot be applied to other cases.

One way of verifying this is to examine $Y_{F,1,1}$, $Y_{F,2,2}$ and $Y_{F,3,3}$, as these entries of Y_F (see figure 3.1.3) each contain the total capacitance of a pn-junction. We will illustrate this for $Y_{F,2,2}$ using figure 3.1.6. In the following we write $Y_F = Y$.

Consider an AC-voltage excitation with amplitude $\hat{u} = 1\text{V}$ at $T1$ while all other ports (see figure 3.1.2) are shorted. The current within the substrate will then flow as qualitatively illustrated in figure 3.1.6.

Now, $Y_{2,5}$ gives us the part of the current that reaches the *backside*. $-Y_{2,5}^{-1}$ can be interpreted as the impedance enclosed by the red boundaries. As illustrated it only contains a part of the distributed pn-junction capacitance at $T1$.

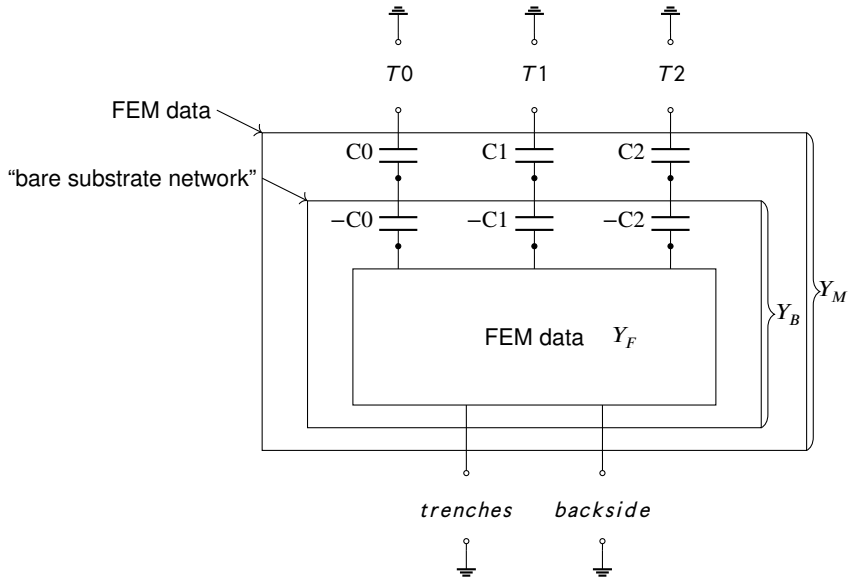


Figure 3.1.5: Equivalent transform of the Y-parameter matrix Y_F obtained from the FEM simulation.

Similarly, $Y_{2,5} + Y_{2,1} + Y_{2,3}$ gives us the current flowing within the area enclosed in blue[4], reaching the *backside*, $T0$ and $T2$. The impedance of this domain represented by $(-Y_{2,5} - Y_{2,1} - Y_{2,3})^{-1}$ also only contains a part of the total distributed capacitance.

On the other hand, the current reaching the *backside*, $T0$, $T2$ as well as the *trenches* flows in the domain highlighted in orange. The impedance represented by this domain accounts for the entire pn-junction capacitance. The current flowing inside this region is given by $Y_{2,5} + Y_{2,1} + Y_{2,3} + Y_{2,4}$ which equals to $-Y_{2,2}$ (see section 2.4.2). Hence, the impedance, this current flows through is given by $Y_{2,2}^{-1}$. For low frequencies the capacitive part of this impedance is dominant over the resistive. Therefore, for low frequencies the following condition has to apply, for our parallel plate capacitor model to be reasonable:

$$Y_{2,2}(f) \approx i2\pi f \epsilon_0 \epsilon_{pn} \frac{d}{h_{pn}}$$

As a matter of fact, we found an excellent agreement with the above condition in verifying this.

3.1.4 Results for the parasitic substrate circuit model

We will now examine the entries of the bare substrate Y-parameter matrix Y_B, we obtained from connecting the negative capacitors to Y_F (section 3.1.3). Part of our examination will be the phase of the resistors which, ideally, should be zero, however we regard a deviation within 45° reasonable. Furthermore, we will look at their dependance on both the frequency f and the distance d. These dependencies can be observed in a plot we provide for each resistor. This plot for the resistors of which the dependencies are trivial or negligible can be found in the appendix of this work. A dependance on d is expected for some of these

[4]Strictly speaking, some of this current also reaches the outer trenches. We neglect this as this current is negligibly small.

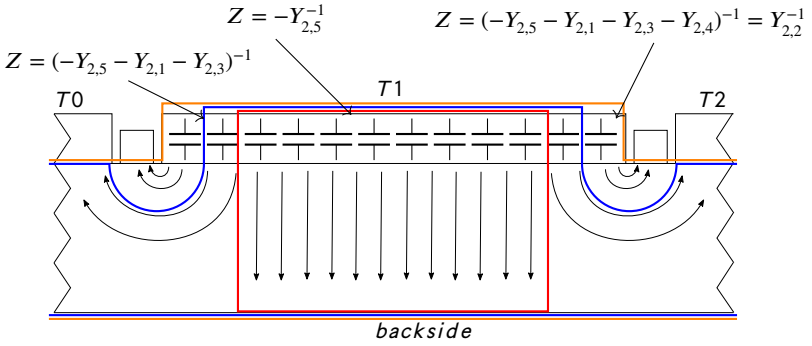


Figure 3.1.6: Qualitative current flow for an AC-voltage excitation at $T1$.

resistors. We regard it reasonable to approximate deviations with respect to f smaller than 3 dB as constant.

In our appendix (section A.2) some field plots are provided in which can be observed that the frequency dependance of these resistors is tied to the change of the current path within the bare substrate.

Theoretically, for our parasitic substrate circuit to fulfil its purpose, all the resistors together have to satisfy our demands on being reasonably close to a real resistor in the same frequency range. However, in section 3.1.5 we will see that for the transfer function from $T0$ to $T2$ we can, depending on d and f, omit some of the resistors.

Table 3.1.1 provides some characteristic quantities by which the extend to which the resistors change with respect to d and f can be evaluated.

R0B, R2B The first two resistors of our parasitic substrate circuit (see figure 3.1.4) we will look at are R0B and B2B (equal by symmetry, see figure 3.1.2). Their values are unaffected by both varying the distance d and frequency. Since they connect the substrate surface underneath $T0$ or $T2$ with the $backside$, they can be described by a simple resistor model. Using for their length h and a width that equals the length l of the buried layer fractions $T0$ or $T2$, the value of these resistors can be calculated by hand, using the substrate conductivity σ, using the equation:

$$\mathrm{R0B} = \mathrm{R2B} = \frac{1}{\sigma}\frac{h}{l} \quad [\Omega\mu\mathrm{m}] \tag{3.1.1}$$

In fact, this approximation is in excellent agreement with the results from Y_B (see appendix, figure A.1.3).

R1B The resistor $R3$, connecting the surface of the substrate underneath $T1$ to the $backside$ can be computed by the same formula as R0B and B2B. Only in this case the reciprocal value of R1B changes linearly with d (see appendix, figure A.1.4).

$$\mathrm{R1B} = \frac{1}{\sigma}\frac{h}{d} \quad [\Omega\mu\mathrm{m}] \tag{3.1.2}$$

By regarding our simulation model (figure 3.1.2), this is in contrast to our initial guess, as we would have expected an occurance of fringe fields to cause a deviation of this model for small d.

RTB The next resistor in discussion is RTB, which connects the *trenches* terminal to the *backside* terminal. This resistor is, as expected by examining figure 3.1.2 largely unaffected by d, and its reciprocal value can be approximated to $1.6(1)\times10^{-6}\,\frac{1}{\Omega\mu m}$ (see appendix, figure A.1.5). Moreover, the frequency dependance of RTB is negligibly small, and its corresponding entry in Y_B is equal to the one in Y_F since they should not be affected by the connection of the negative capacitors. In section 3.1.5 we will see, however, that this resistor does not play a significant role in describing couplings between $T0$ and $T2$, and can therefore be neglected in our parasitic substrate circuit.

R0T, R2T The resistors R0T and R2T (equal by symmetry, see figure 3.1.2) show, for frequencies $f > 100$MHz, a strong dependance on f. For $d = 50\,\mu$m an increase of its reciprocal value by 7.1 dB can be observed within the frequency domain [10 MHz, 1 GHz]. Their dependance on d is, especially for $f > 100$ MHz negligible. It can also be observed that the phase deviates from zero within the mid frequencies [100 MHz, 1 GHz] but stays within our demands. As RTB, these resistors too can, as we will see in section 3.1.5, be neglected in our parasitic substrate circuit.

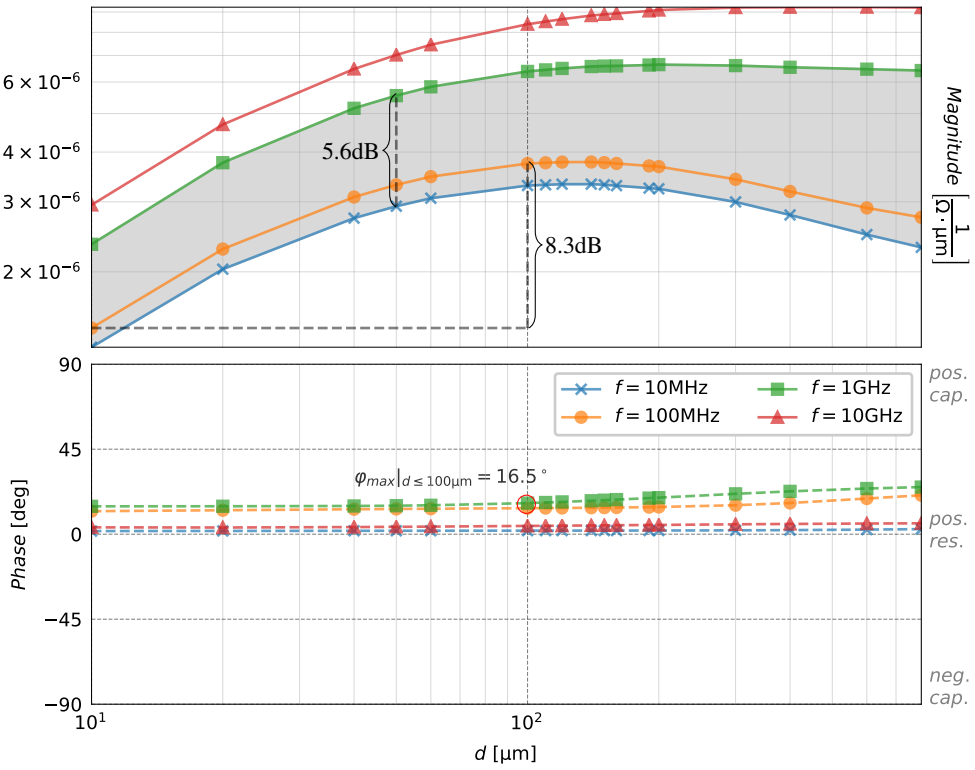


Figure 3.1.7: Distance dependance of the magnitude and phase of $R01^{-1}$ and $R12^{-1}$ for different frequencies.

R01, R12 The frequency and distant dependant reciprocal value of R01 and R12 (equal by symmetry, see figure 3.1.2) obtained from the respective entry of Y_B is illustrated in figure 3.1.7. Their dependance on d is notably larger for distances $d < 100\,\mu m$, whereas for $d > 100\,\mu m$ $\frac{dR01}{dd}$ is much smaller. Apparently, for small d when $T0$ is excited with an AC-voltage more current paths terminate in $T2$, which leads to less current at $T1$. In the limit of large d, on the other hand, for a voltage excitation at $T0$ the current flowing through R01 does not reach $T2$ because all of it is absorbed by $T1$, and hence the current at $T1$ will stay constant.

A slight deviation from zero of the phase is notable in the mid frequencies [100 MHz, 1 GHz] which for our demands is negligible. Moreover, in closely examining figure 3.1.7 we find that in the frequency domains [10 MHz, 100 MHz] and [1GHz, 10GHz] the impedance can, for any particular d, be well approximated to a constant value. A frequency dependant change of impedance is more significant within the frequencies [100 MHz, 1 GHz].

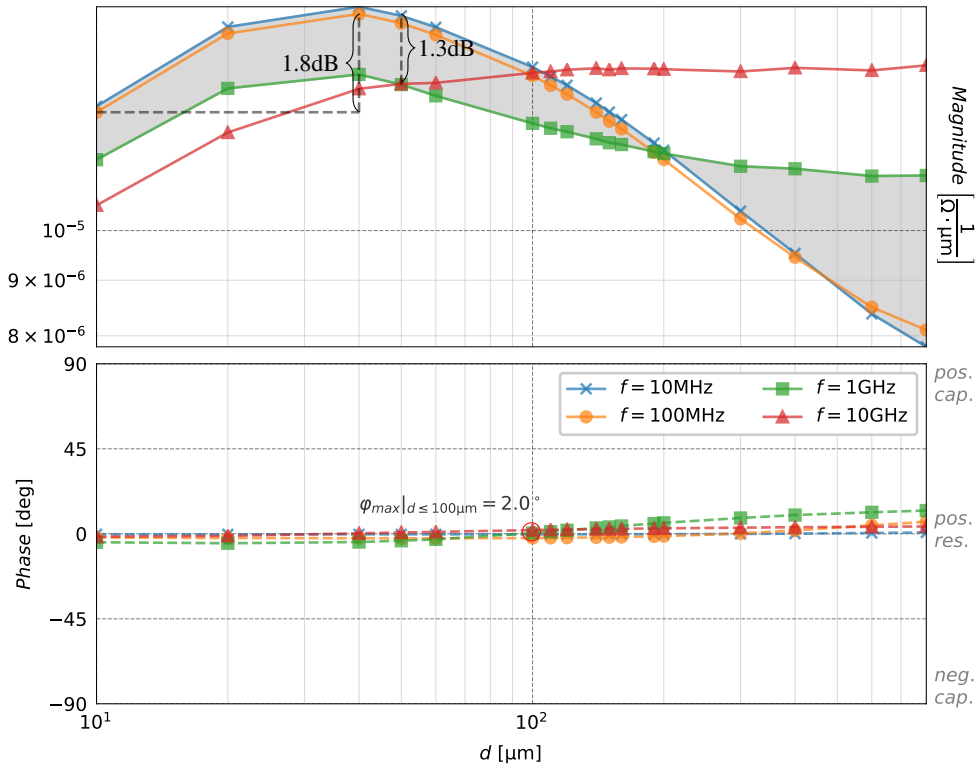


Figure 3.1.8: Distance dependance of the magnitude and phase of $R1T^{-1}$ for different frequencies.

R1T As shown in figure 3.1.8 the resistor R1T connecting the substrate surface underneath $T1$ to the *trenches* terminal is, particularly for $d < 100\,\mu m$, mostly unaffected by a variation of d and f. For $d > 100\,\mu m$ and $f < 1\,GHz$, a distance and frequency dependance is more notable. For $f > 1\,GHz$ the dependance of R1T on d or f is negligible. We will see in

section 3.1.5 that this resistor is important in the transfer function from $T0$ to $T2$ for distances $d \geq 400\,\mu\text{m}$, for small distances neglecting R1T is reasonable.

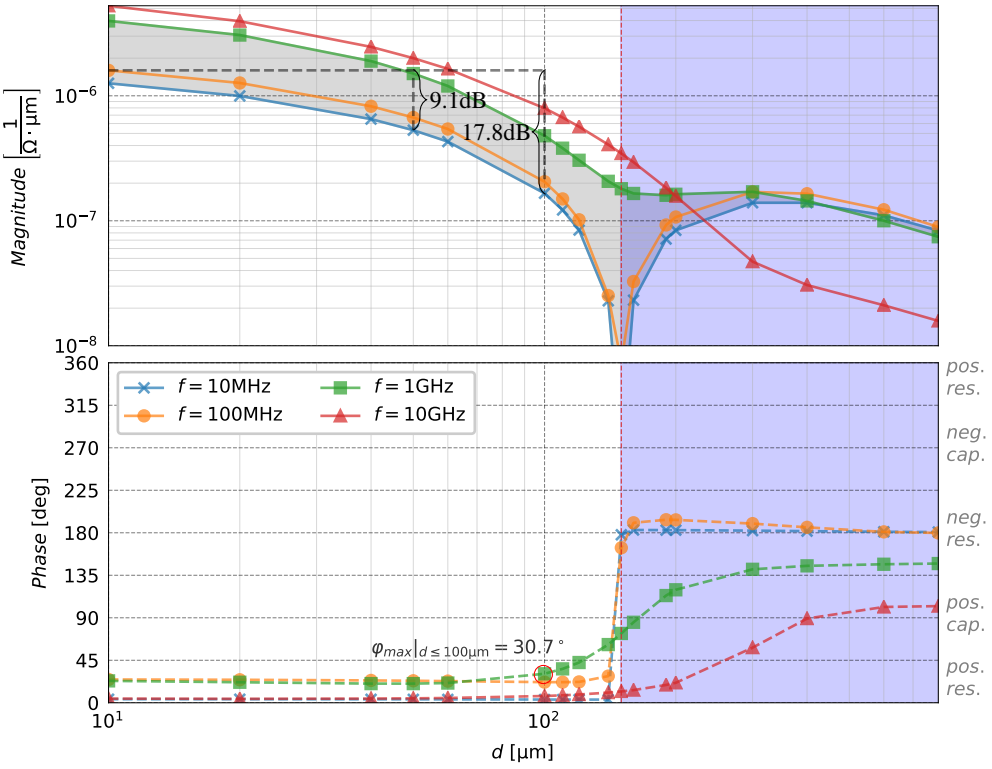


Figure 3.1.9: Distance dependance of the magnitude and phase of R02^{-1} for different frequencies. For $d \geq 150\mu\text{m}$ (indicated in blue), R02^{-1} is real and negative for $f \in \{10\text{MHz}, 100\text{MHz}\}$.

R02 The resistor R02 which represents the two-terminal impedance between $T0$ and $T2$ in our bare substrate network Y_B plays, as we will see in section 3.1.5, a very important role our parasitic substrate circuit (figure 3.1.4). Its dependencies on f and d are illustrated in figure 3.1.9. A pronounced local minimum of the absolute reciprocal value of R02 can be observed for $d = \frac{3}{4}h = 150\,\mu\text{m}$ at frequencies $f = 10\,\text{MHz}$ and $f = 1\,\text{GHz}$. In examining the phase of R02, this can be traced back to a zero crossing of the resistance. For higher frequencies the same, however less abrupt trend is visible.

For $d < 100\,\mu\text{m}$ the phase at 10 MHz and 10 GHz is approximately zero, however in between these frequencies a discrepancy is notable. Yet its maximum value does not exceed 45° (see appendix, figure A.1.1) which stays in agreement with what we regard reasonable.

The decrease of its reciprocal value, which is an increase of R02, with increasing d seems intuitive as this implies weaker couplings between $T0$ and $T2$ for larger distances. For $d < 150\,\mu\text{m}$ the magnitude of R02 seems to monotonically increase with f.

At this point we cannot make well reasoned assumptions on how the properties of R02 for $d > 150\,\mu m$, which in figure 3.1.9 is indicated in blue, can be interpreted. Unlike for $d < 150\,\mu m$, a pattern in its frequency dependance is less easy to find. For $f < 1\,GHz$ the phase of R02 is close to 180° which can be interpreted as a negative resistor. Theoretically, the presence of a negative resistor in our parasitic substrate circuit should not stand in the way of its purpose as negative resistors are just as easy to implement in circuit simulations as regular ones. On the other hand, a steady increase of the absolute value of R02 points to the possibility that R02 is not important for large d. In fact, as we will describe in section 3.1.5, the relevance of these properties of R02 are difficult to pin down, and a complete and sound procedure to determine how important these properties are is beyond the scope of our work.

R	$\frac{Y_{max}}{Y_{min}}$ [a]	$20\log\frac{Y_{max}}{Y_{min}}$ [a]	$\frac{Y_{max}}{Y_{min}}$ [b]	$20\log\frac{Y_{max}}{Y_{min}}$ [b]	φ^c_{max}	eq./value[d]	figure
R02	$\frac{1.60\times10^{-6}}{2.05\times10^{-7}}$	17.8dB	$\frac{1.51\times10^{-7}}{5.31\times10^{-6}}$	9.1dB	30.7°		3.1.9
R01, R12	$\frac{3.74\times10^{-6}}{1.44\times10^{-6}}$	8.3dB	$\frac{5.55\times10^{-6}}{2.92\times10^{-6}}$	5.6dB	16.5°		3.1.7
R0T, R2T	$\frac{3.46\times10^{-6}}{2.61\times10^{-6}}$	2.4dB	$\frac{5.21\times10^{-6}}{2.30\times10^{-6}}$	7.1dB	21.4°		A.1.2
R1T	$\frac{1.58\times10^{-5}}{1.29\times10^{-5}}$	1.8dB	$\frac{1.58\times10^{-5}}{1.36\times10^{-5}}$	1.3dB	2.0°		3.1.8
RTB						$1.6(1)\times10^{-6}$	A.1.5
R0B, R2B						$\sigma\frac{l}{h}$	A.1.3
R1B						$\sigma\frac{d}{h}$	A.1.4

[a] for $f = 100MHz$, $d \in [10\mu m, 100\mu m]$ (distance dependance)
[b] for $f = [10MHz, 1GHz]$, $d = 50\mu m$ (frequency dependance)
[c] for $d \in [10\mu m, 100\mu m]$
[d] $\left[\frac{1}{\Omega\mu m}\right]$

Table 3.1.1: Overview of the frequency and distance dependance of the resistors in the bare substrate network shown in figure 3.1.4.

From the resistor results presented in this section we can draw the conclusion that for $d < 150\,\mu m$ and $10\,MHz \leq f \leq 100\,MHz$ is possible to predict a reasonably accurate value for substrate couplings using our parasitic substrate circuit (figure 3.1.4). For $f > 10\,MHz$ larger errors have to be expected as the frequency dependance for the resistors R10, R12 and R02 accounts for considerably more than 3 dB. The prediction of substrate couplings for $d < 150\,\mu m$ depends on whether the resistor R02 can be implemented as a negative resistor in our parasitic substrate circuit, or even be completely omitted. This will be discussed in section 3.1.5.

3.1.5 Determining the relevance of the resistors with respect to the transfer function from T0 to T2

In this section we will try to evaluate the importance of each resistor in our parasitic substrate circuit (figure 3.1.4) with respect to the transfer function from $T0$ to $T2$. To obtain the transfer function from $T0$ to $T2$ of our parasitic substrate circuit (figure 3.1.4), we will short all ports, except for $T0$, where we will apply a voltage source. We will then measure the current at $T2$. By shorting most of the ports we can combine many parallel impedances as shown in

3.1.10 (left). To avoid an excessive use of fractions we will use the letter "G" to indicate the conductance 1/R such that for instance R0B‖R0T is given by:

$$\mathrm{R0B} \parallel \mathrm{R0T} = \frac{1}{\mathrm{G0B} + \mathrm{G0T}}$$

To eliminate node N3 we will use the Y-Δ-transform (see section 2.4.3) of the subcircuit highlighted by the dashed rectangle. The values of the impedances of the resulting Δ-subcircuit are then given by (see section 2.4.3):

$$\mathrm{R1M} = \frac{\mathrm{G01} + \mathrm{G12} + \mathrm{G1B} + \mathrm{G1T} + i\omega\mathrm{C1}}{\mathrm{G01} \cdot \mathrm{G12}} \tag{3.1.3}$$

$$\mathrm{R0M} = \frac{\mathrm{G01} + \mathrm{G12} + \mathrm{G1B} + \mathrm{G1T} + i\omega\mathrm{C1}}{\mathrm{G01} \cdot (\mathrm{G1B} \cdot \mathrm{G1T} + i\omega\mathrm{C1})} \tag{3.1.4}$$

$$\mathrm{R2M} = \frac{\mathrm{G01} + \mathrm{G12} + \mathrm{G1B} + \mathrm{G1T} + i\omega\mathrm{C1}}{\mathrm{G12} \cdot (\mathrm{G1B} \cdot \mathrm{G1T} + i\omega\mathrm{C1})} \tag{3.1.5}$$

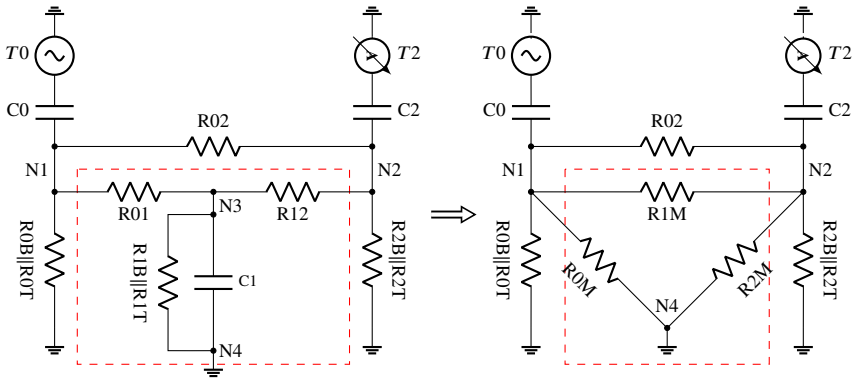


Figure 3.1.10: Obtaining the transfer function from $T0$ to $T2$

Now, to derive an analytical formula that gives us the current at $T2$ for an AC-voltage excitation of amplitude $\hat{u}_{T0}$ at $T0$, we will assume that the voltage delivered at N1 from the voltage divider formed by the series connection of C2 and R0B‖R0T‖R0M(f) is unaffected by the load represented by the subcircuit connected at N1. To obtain the current at N3, we will assume that the voltage drop between N1 and N3 is equal to that over R0B‖R0T‖R0M(f). The current at $T2$ is equal to that over C2 which can be obtained from the current over R1M and the current divider at N3 formed by C2 and R0B‖R0T‖R0M(f). The current at $T2$ is then given by:

$$I_{T0\to T2} \approx \hat{u}_{T0} \cdot \underbrace{\frac{\frac{1}{\mathrm{G0B+G0T+G0M}}}{\frac{1}{\mathrm{G0B+G0T+G0M}} + \frac{1}{i\omega\mathrm{C0}}}}_{\text{voltage divider}} [\mathrm{G1M} + \mathrm{G02}] \underbrace{\frac{i\omega\mathrm{C2}}{i\omega\mathrm{C2} + \mathrm{G2B} + \mathrm{G2T} + \mathrm{G2M}}}_{\text{current divider}} \tag{3.1.6}$$

From the results we obtained in section 3.1.4 we observe that

$$\mathrm{G0B} = \mathrm{G2B} \gg \mathrm{G0T} = \mathrm{G2T} > \mathrm{G0M} = \mathrm{G2M},$$

and we can therefore neglect G0T, G0T and G0M, G2M in the current and voltage divider. For G02 we will use the the frequency dependant data from Y_B, the values for G0B and G2B on the other hand can be obtained by equation 3.1.1, and the value for G1B by equation 3.1.2.

The transfer function from $T0$ to $T2$ in our FEM Y-parameter matrix Y_F is represented by $-Y_{F,1,3} = -Y_{F,3,1}$ (see figure 3.1.3). Our analytical approximation for it is given by:

$$Y_{T0\to T2} = \frac{I_{T0\to T2}}{\hat{u}_{T0}}$$

As this will help us in the following, we will now subdivide our transfer function in four parts, *a b*, *c* and *e*, as illustrated in equation 3.1.7:

$$Y_{T0\to T2} \approx \underbrace{\frac{\mathrm{R0B}}{\mathrm{R0B} + \frac{1}{i\omega \mathrm{C0}}}}_{a} [\underbrace{\mathrm{G1M}}_{b} + \underbrace{\mathrm{G02}}_{c}] \underbrace{\frac{i\omega \mathrm{C2}}{i\omega \mathrm{C2} + \mathrm{G2B}}}_{e} \tag{3.1.7}$$

In the following, we will examine the properties of $-Y_{F,1,3}$. Moreover we will use $-Y_{F,1,3}$ to determine whether our analytical approximation is valid, and if we can make further approximations.

In the transfer function represented by $-Y_{F,1,3}$ we observe for low frequencies a quadratic asymptotic, as illustrated in figure 3.1.11 by red, dashed lines.

For small f we can approximate equation 3.1.7 and obtain this quadratic asymptotic:

$$Y_{T0\to T2}(f_{small}) = -\mathrm{R0B}\,\mathrm{R2B}\,\mathrm{C1}\,\mathrm{C2}\,\omega^2 \cdot \mathrm{G02} \cdot \mathrm{G1M0} \tag{3.1.8}$$

where

$$\mathrm{G1M0} = \mathrm{G1M} \cdot i\omega \mathrm{C1}$$

Moreover, the negative sign in equation 3.1.8 explains the 180° asymptotic in the transfer functions phase for low frequencies (see figure 3.1.11).

Transfer function from T0 to T2 for small d Our guess is that for small d the current at $T1$ is much smaller than that at $T2$. By neglecting $T1$ completely, G1M vanishes in equation 3.1.7 which then simplifies to:

$$Y_{T0\to T2} \approx a \cdot c \cdot e \tag{3.1.9}$$

We have seen that for distances $d \leq 60\,\mu\mathrm{m}$ equation 3.1.9 is a very reasonable approximation. This is illustrated in figure 3.1.11 where results of which and the simulation data from Y_F show a good agreement.

Transfer function from T0 to T2 for large d We have observed that for larger distances $d > 60\,\mu\mathrm{m}$ equation 3.1.9 loses its validity. This means, the influence of $T1$ is more important here. Thus, for $d > 60\,\mu\mathrm{m}$ the only approximation we could still make are with respect to G1M. For now, we will use equation 3.1.7 as it is. As described in section 3.1.4, the properties of the resistor R02 we obtained from Y_B are difficult to interpret, for $d > 150\,\mu\mathrm{m}$. In the following, we will try to classify R02 with respect to its relevance for the transfer function from $T0$ to $T2$. We will approach this by comparing $-Y_{F,1,3}$ with equations 3.1.7, 3.1.9 and

$$a \cdot b \cdot e. \tag{3.1.10}$$

Let us first regard the results we obtain for $d = 100\,\mu\mathrm{m}$.

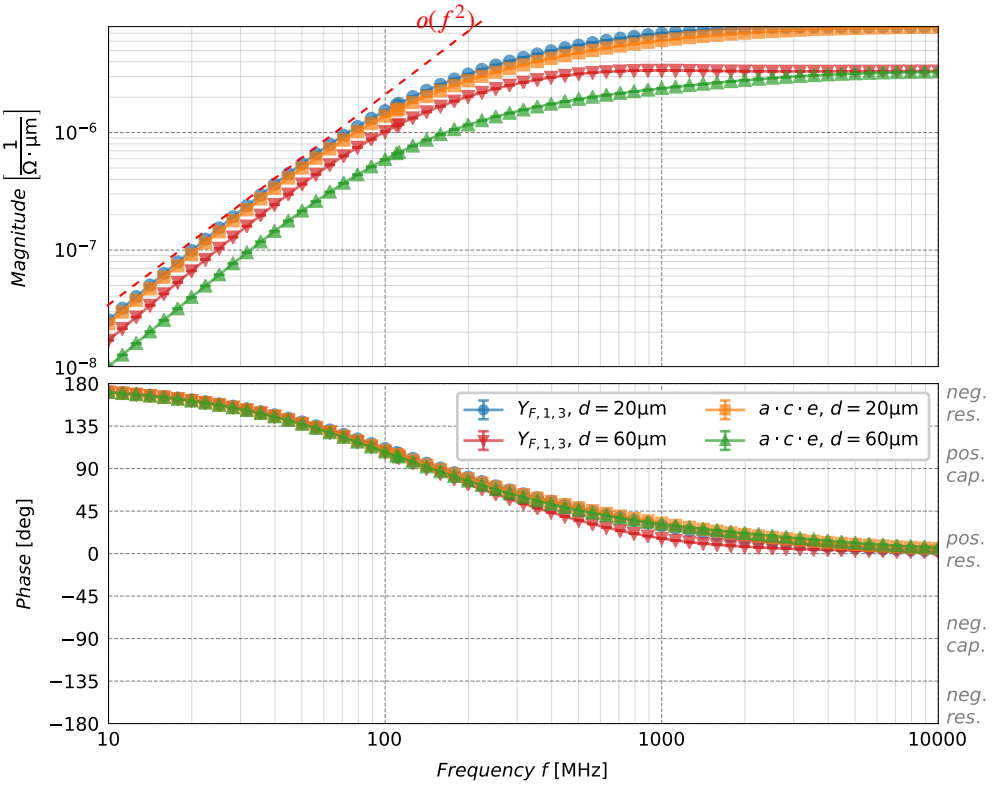


Figure 3.1.11: Transfer function for small d

In figure 3.1.12, we can see that the approximation we made for $d \leq 60\,\mu m$ is not as good for larger d except for $f > 1\,GHz$. On the other hand equation 3.1.10 in which R02 is completely neglected is for $f < 1\,GHz$ in good agreement with the exact transfer function $Y_{F,1,3}$ but not for $f > 1\,GHz$.

For $d = 400\,\mu m$ something completely different happens. The magnitude of $a \cdot b \cdot e$ and $a \cdot c \cdot e$ are nearly the same, however their phases differ by approx. 180° which can be seen in figure 3.1.13. In section 3.1.4 we have seen that in the lower frequency domain the phase of R02 abruptly changes by approx. 180° for $d > 150\,\mu m$. We can see now that having this negative resistor in our parasitic substrate circuit harms its essential purpose. That is, the transfer function from $T0$ to $T2$, as we can see in figure 3.1.13, is defined by a difference of two values which is notably smaller than the values itself.

We will illustrate the significance of this so-called cancellation effect using a simple example. Let us assume we fix the values for G1M(f) and G02 with an error of $0.05 \cdot |G1M|$ and $0.05 \cdot |G02|$ respectively. Moreover, we assume that

$$\Delta = GM1 + G02 \approx 0.1 \cdot |G02|.$$

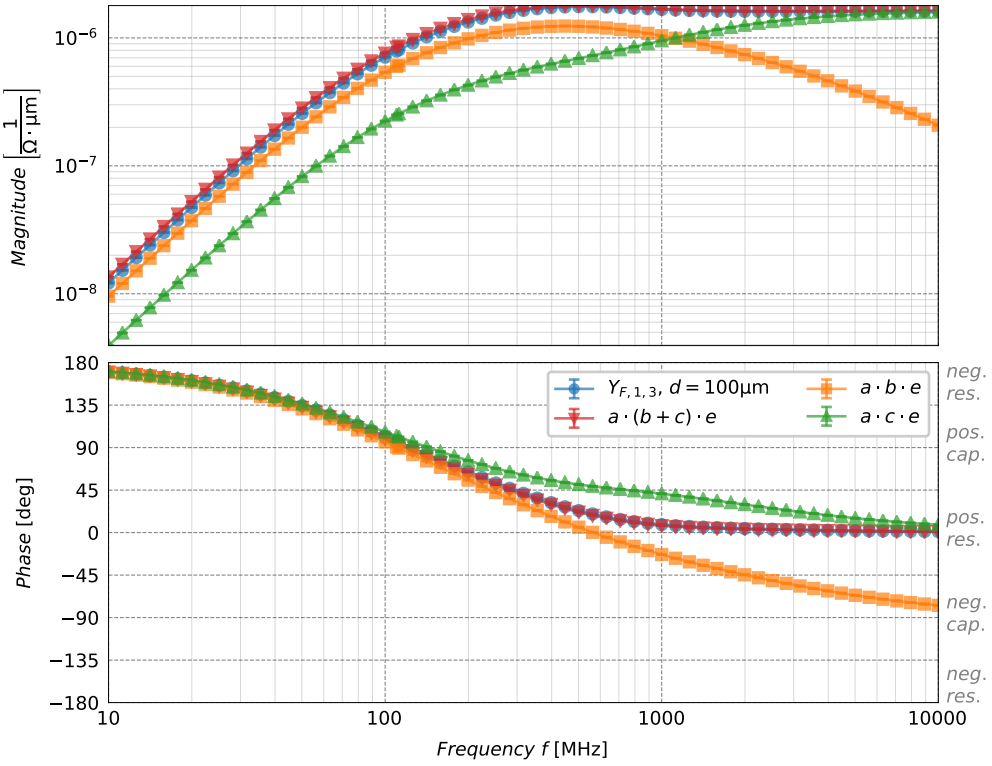


Figure 3.1.12: Transfer function for $d = 100\mu m$

Using Gaussian error propagation the error of the above equation is given by:

$$\begin{aligned}\sigma_\Delta &= \sqrt{(0.05 \cdot \mathrm{G1M})^2 + (0.05 \cdot \mathrm{G02})^2} \\ &= \sqrt{(0.05 \cdot 1.1 \cdot \mathrm{G02})^2 + (0.05 \cdot \mathrm{G02})^2} \\ &\approx \sqrt{2 \cdot 0.05^2}|\mathrm{G02}| \approx 0.07 \cdot |\mathrm{G02}|\end{aligned}$$

Hence, the error of Δ has a value that is approximately 70% of Δ itself. Using this value to obtain a reasonable approximation for the transfer function from $T0$ to $T2$ is therefore practically not possible. Nonetheless, as will be shown in the following, even for some distances which are beyond 150µm it is possible to omit R02 and still obtain a reasonable value for $Y_{T0 \to T2}$ in the frequency domain [10MHz, 1GHz].

Reducing parasitic substrate circuit As we have seen in the preceding paragraphs, not all the resistors in our parasitic substrate circuit (figure 3.1.4) are always relevant to obtain adequate results for the coupling between $T0$ and $T2$. Here, we will use the following criteria to determine a simplified model of that depicted in figure 3.1.4 for different values for d and

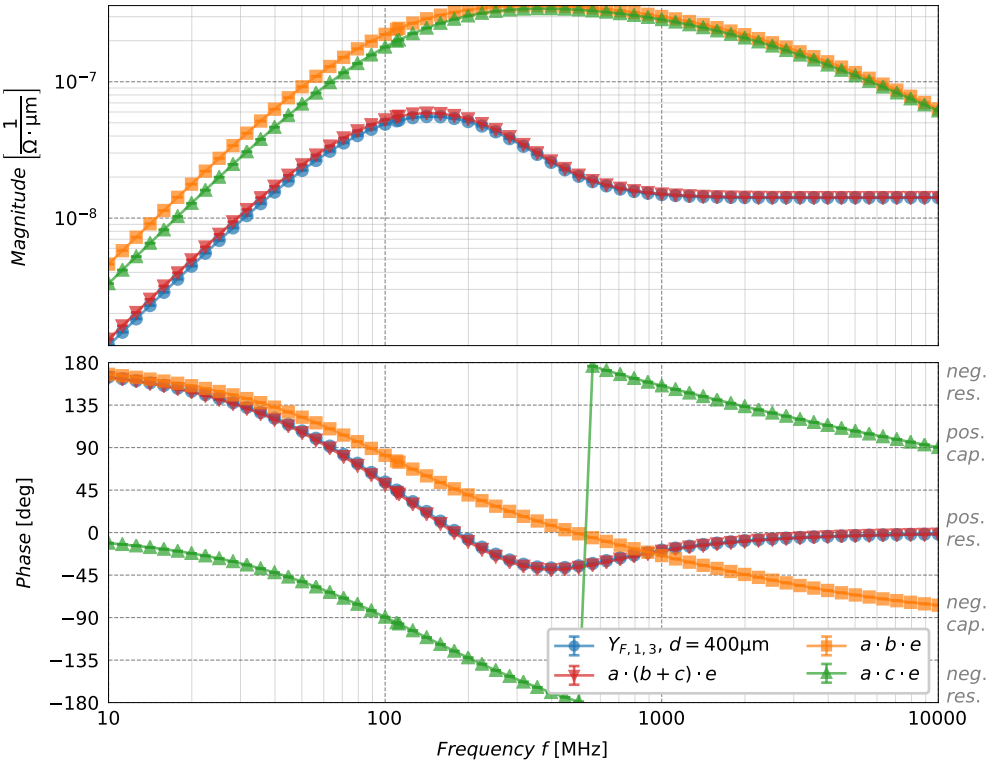


Figure 3.1.13: Transfer function for $d = 400\mu m$

different domains for f:

$$\left|20 \log \frac{Y_{F,1,3}}{Y_{T0\rightarrow T2,\text{simplified}}}\right| < 6\text{dB} \tag{3.1.11}$$

and

$$|\arg(Y_{F,1,3}) - \arg(Y_{T0\rightarrow T2,\text{simplified}})| < 45° \tag{3.1.12}$$

The simplified circuit models we found for these criteria are shown in table 3.1.2.

From the result presented in table 3.1.2 we can see that the cancellation effects caused by the resistor R02 for $60\,\mu m < d \leq 200\,\mu m$ and $10\,MHz \leq f < 1\,GHz$ do not play a very significant role as for these values for f and d R02 can be omitted. Hence, predictions of substrate couplings using our parasitic substrate circuit are still possible for distances up to 200 µm and frequencies up to 1 GHz.

3.1.6 Generalization of the simulation results for different pn-junction capacitance and substrate height

In section 2.3 we have derived the PDE for which is solved to obtain the electric field within our substrate model and through it the Y-parameter matrix Y_F. In this section, we will try to find out if we can obtain the Y-parameter matrix $Y_{F,h1,c1}$ for a particular substrate height and

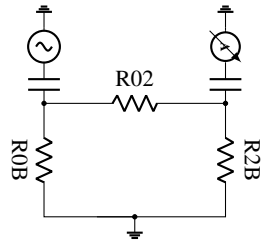
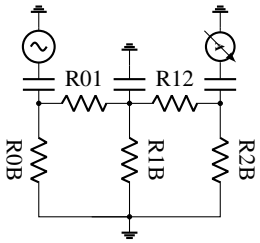
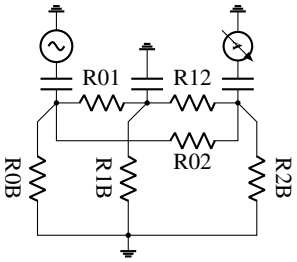
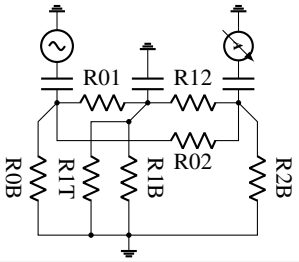
		
$d \leq 60\,\mu\text{m}$, $10\,\text{MHz} \leq f \leq 10\,\text{GHz}$; and $d \leq 100\,\mu\text{m}$, $f > 1\,\text{GHz}$	$60\,\mu\text{m} < d \leq 200\,\mu\text{m}$ $10\,\text{MHz} \leq f < 1\,\text{GHz}$	$d < 400\,\mu\text{m}$ $10\,\text{MHz} \leq f \leq 10\,\text{GHz}$
	$10\,\text{MHz} \leq f \leq 10\,\text{GHz}$ $d \geq 400\,\mu\text{m}$	

Table 3.1.2: Simplifications of the parasitic substrate circuit (figure 3.1.4) for which the transfer function from $T0$ to $T2$ is still reasonably accurate (see equations 3.1.11 and 3.1.12).

pn-junction capacitance per unit area by a simple transormation of an existing Y-parameter matrix $Y_{F,h2,c2}$

Our starting point is equation 2.3.1. For simplicity, we will write:

$$\hat{\sigma}(\vec{r}) = \sigma(\vec{r}) + i\omega\epsilon(\vec{r}) \tag{3.1.13}$$

the equation 2.3.1 writes:

$$0 = \nabla \cdot \left(\hat{\sigma}(\vec{r}) \cdot \nabla\phi(\vec{r})\right) \tag{3.1.14}$$

We are first interested in what happens if we apply a coordinate transformation $\vec{r} = \lambda\vec{r'}$ to 3.1.14. For this we will apply the product rule in 3.1.14:

$$0 = \hat{\sigma}(\vec{r}) \cdot \Delta\phi(\vec{r}) + \nabla\hat{\sigma}(\vec{r}) \cdot \nabla\phi(\vec{r}) \tag{3.1.15}$$

While ∇ is defined as $(\frac{\partial}{\partial r_1}, \frac{\partial}{\partial r_2}, \frac{\partial}{\partial r_3})^T$ we define $\nabla' = (\frac{\partial}{\partial r'_1}, \frac{\partial}{\partial r'_2}, \frac{\partial}{\partial r'_3})^T$. The substitution with $r \to \lambda r'$ then yields:

$$0 = \hat{\sigma}(\lambda\vec{r'}) \cdot \Delta'\phi(\lambda\vec{r'}) + \nabla'\hat{\sigma}(\lambda\vec{r'}) \cdot \nabla'\phi(\lambda\vec{r'}) \tag{3.1.16}$$

From the chain rule it follows that $\nabla'\phi(\lambda\vec{r'}) = \lambda\nabla\phi(\lambda\vec{r'})$, and the above equation simpifies to:

$$0 = \hat{\sigma}(\lambda\vec{r'}) \cdot \cancel{\lambda^2}\Delta\phi(\lambda\vec{r'}) + \cancel{\lambda}\nabla\hat{\sigma}(\lambda\vec{r'}) \cdot \cancel{\lambda}\nabla\phi(\lambda\vec{r'}) \tag{3.1.17}$$

This in turn means that the solution for ϕ is the same in equation 3.1.16 as in equation 3.1.14:

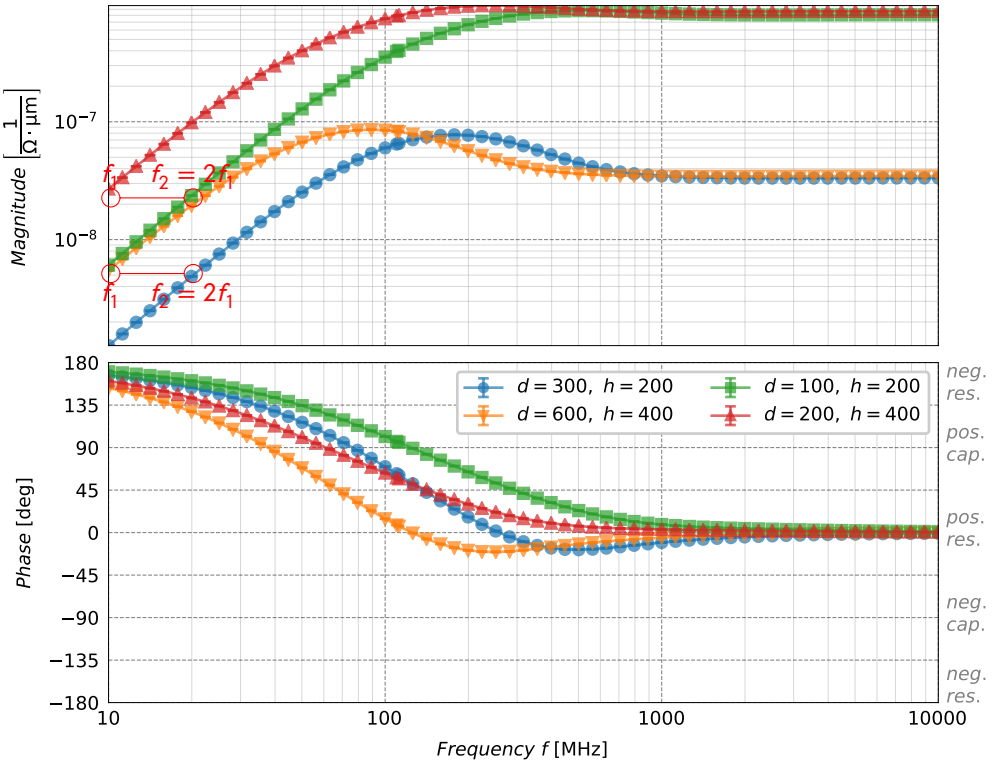


Figure 3.1.14: Simulation results for $\lambda = 1/2$ as illustrate in figure 3.1.15

$$0 = \nabla \cdot \left(\hat{\sigma}(\lambda \vec{r'}) \cdot \nabla \phi(\lambda \vec{r'})\right) = \nabla \cdot \left(\hat{\sigma}(\vec{r}) \cdot \nabla \phi(\vec{r})\right) \tag{3.1.18}$$

Now, let us assume we have the solution for ϕ for a particular set of parameters l, d, h, σ, ϵ, and q. To avoid further indexing we write $q = h_{pn}$. For this solution we will write $\phi_{l,d,h,\sigma,\epsilon,q}(\lambda \vec{r'})$. Then the solution for $\phi(\vec{r'})$ is is given by the solution for a simulation model that is scaled by λ:

$$\phi_{l,d,h,\sigma,\epsilon,q}(\lambda \vec{r'}) \rightarrow \phi_{l/\lambda,d/\lambda,h/\lambda,\sigma,\epsilon,q/\lambda}(\vec{r'})$$

The above solutions for ϕ are not the same but let us have a look at the Y-parameter matrix. Let us compute $Y_{1,3}$, which physically, is the current entering $T0$ normalized by the AC-voltage excitation amplitude $\hat{u}_{T2}$ at $T2$ (see figures 3.1.3 and 3.1.2). For simplicity, we will assume that $\hat{u}_{T2} = 1\text{V}$ and $\sigma = 1$, and to reduce the number of indices we write $Y_{1,3} = Y$:

$$
\begin{aligned}
Y_{l,d,h,\sigma,\epsilon,q} = \frac{I_{T0}}{\hat{u}_{T2}} &= \int_{T0} \left(\frac{\mathrm{d}}{\mathrm{d}z} \phi_{l,d,h,\sigma,\epsilon,q}(\vec{r}) \right) \mathrm{d}x \\
&= \int_{T0/\lambda} \left(\frac{\mathrm{d}}{\mathrm{d}z} \phi_{l,d,h,\sigma,\epsilon,q}(\lambda \vec{r'}) \right) \lambda \mathrm{d}x' \\
&= \int_{T0/\lambda} \Big(\frac{\mathrm{d}}{\mathrm{d}z} \underbrace{\phi_{l,d,h,\sigma,\epsilon,q}(\vec{r'})}_{\phi_{l/\lambda,d/\lambda,h/\lambda,\sigma,\epsilon,q/\lambda}(\vec{r'})} \Big) \frac{1}{\lambda} \lambda \mathrm{d}x' \\
&= Y_{l/\lambda,d/\lambda,h/\lambda,\sigma,\epsilon,q/\lambda}
\end{aligned} \tag{3.1.19}
$$

Hence, scaling the complete model will not change the Y-parameter $Y_{1,3}$. We are however only interested in the result for scaling h and ϵ. We can make the following reasonable approximations: With $C \approx \epsilon \frac{l}{q}$ we can write $\epsilon, q/\lambda \rightarrow q, \lambda\epsilon$, and since $l \approx \infty$ we can write $l/\lambda \rightarrow l$. This gives:

$$
Y_{l/\lambda,d/\lambda,h/\lambda,\sigma,\epsilon,q/\lambda}(\vec{r'}) \approx Y_{l,d/\lambda,h/\lambda,\sigma,\lambda\epsilon,q}(\vec{r'}) \tag{3.1.20}
$$

Now, not scaling q but inversely scaling ϵ will not change the Y-parameter. However, scaling ϵ only will have a frequency shift in equation 3.1.13:

$$
\hat{\sigma} = \sigma(\vec{r}) + i \underbrace{\omega\lambda}_{\text{frequency shift}} \epsilon(\vec{r}) \tag{3.1.21}
$$

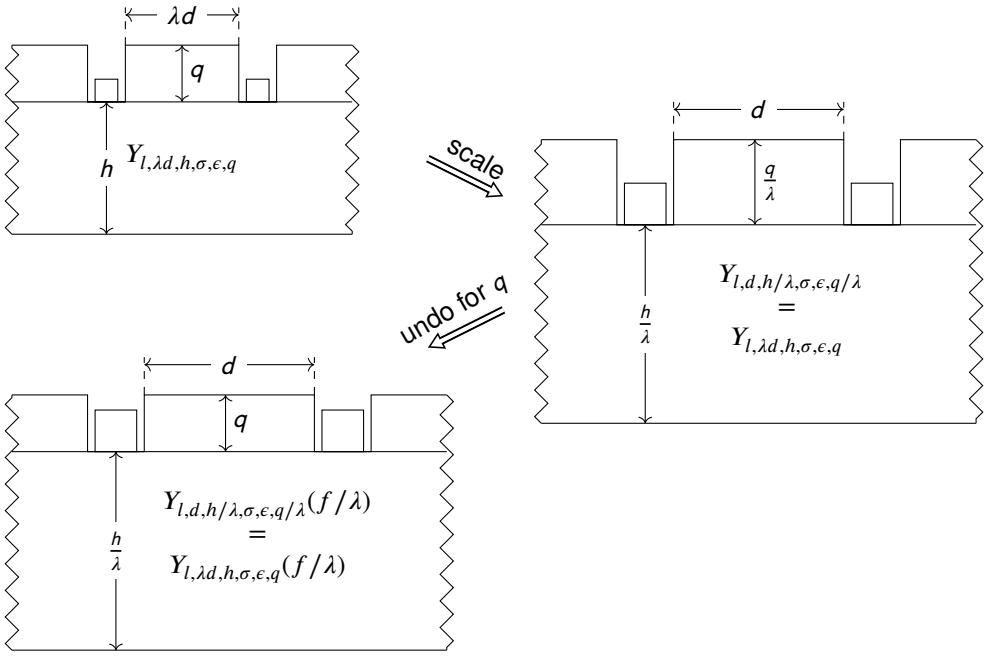


Figure 3.1.15: Obtaining the Y-parameters for different substrate heights

Hence, the conclusion from our above derivation we can draw is on one hand, that scaling the pn-junction capacitance would mean a different value for ϵ with the result of a frequency

shift in our data. The procedure for obtaining the result from scaling h is illustrated in figure 3.1.15. To obtain $Y_{d,h/\lambda}$ the starting point is $Y(d/\lambda, h)$. Scaling the complete model by λ results in the desired value for h, q on the other hand is scaled too. This does not change $Y_{1,3}(d/\lambda)$. However, by scaling back q which equals scaling ϵ our data shifts in frequency.

The the above derivation of this symmetry transformation would also imply a scaling of the trenches. As shown in figure 3.1.14, for $\lambda \geq \frac{1}{2}$ neglecting this is very reasonable.

3.1.7 Trench to trench impedance comparison with measured data

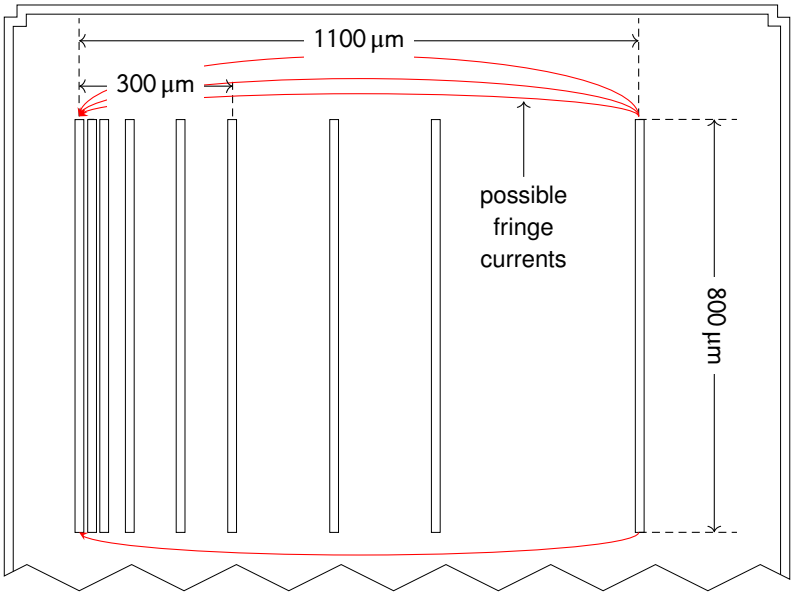


Figure 3.1.16: Test chip from which the trench to trench impedance measurements illustrated in figure 3.1.17 were obtained.

Our group has made trench to trench impedance measurement on a test chip as illustrated in figure 3.1.16. To verify that our FEM substrate model produces reliable results, we will briefly compare the measurement data with the trench to trench impedance in our model. In the measurement, the backside of the test chip was unconnected, and the substrate height of the test chip was 300µm. Therefore we will re-simulate our FEM model, only now we will leave out the backside contact, distinguish between the different trenches and set the height h to be 300µm (see figure 3.1.2). As illustrated in figure 3.1.16 the lateral length of the trenches on the test chip used for the measurement is 800 µm. For our comparison we will convert the 2D FEM data appropriately to the measurement. The measurement was made at a frequency $f = 1$ KHz, however it should be noted that the frequency should not have an impact on the measured impedance.

The results we obtained are illustrated in figure 3.1.17. It can be said that the results from our FEM simulation are in very good agreement with the measurements. A possible explanation for an average discrepancy of 1dB can be the occurrence of lateral fringe fields in the measurement. In the simulation we can observe an increase of the slope for $d > 300\,\mu$m. Our guess is that for large d the impedance increases linearly with d, whereas for small d a curvature of the current path is more dominant.

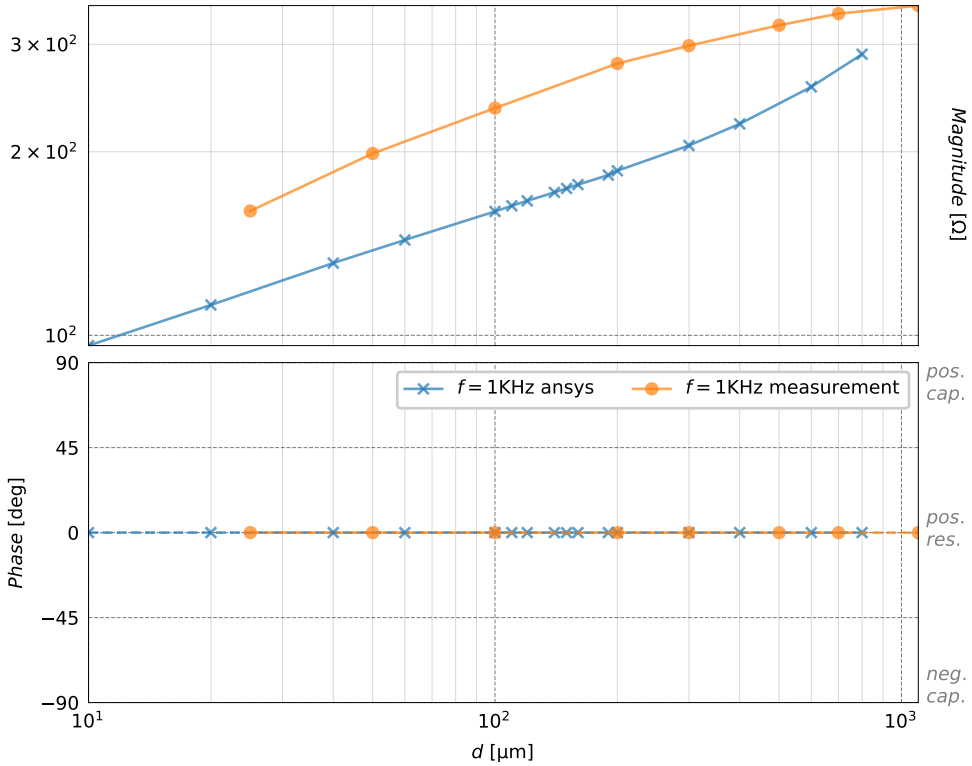


Figure 3.1.17: Trench to trench impedance comarison of measurement and 2D FEM simulation results for $h = 300\,\mu m$

3.2 Evaluation of Substrate Extraciton Tools

3.2.1 3D Test Layout, Y-parameter simulation and computation of discrete modelresistors

The substrate extraction tools we will evaluate (section 3.2.2 and 3.2.3) are built to extract the substrate of a 3D layout. Therefore, we require a new 3D model the results from which can be compared with our 2D FEM data. Theoretically, the 3D model that comes the closest to our 2D model is represented by the same 2D model only stretched in z-direction by a distance that is virtually infinitely long. As we are unable to predict the relevance of boundary effects that occur in such a model that is still of dimensions that the parasitic extraction solvers can handle, we will go for a different model.

A slightly different model in which the substrate couplings are still comparable to our 2D FEM model to a reasonable extent is represented by a concentric layout, which is illustrated in figure 3.2.1.

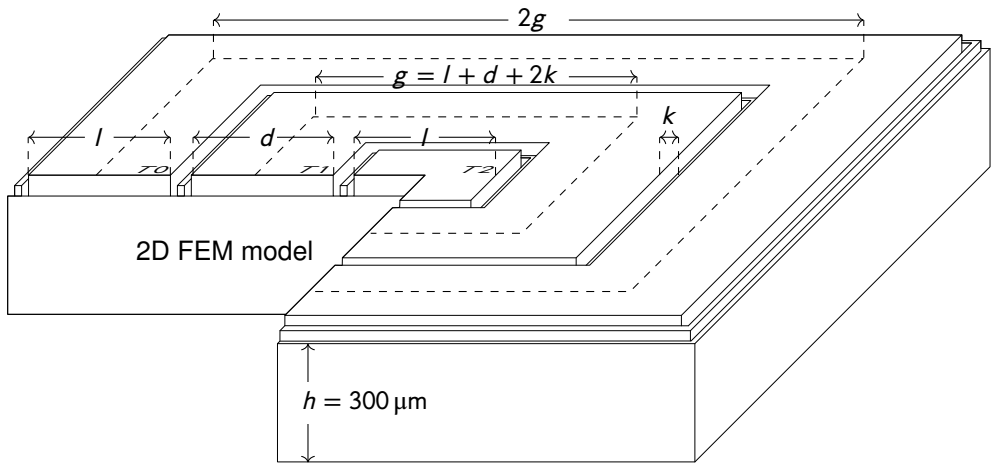


Figure 3.2.1: Concentric 3D test layout in analogy to the 2D FEM model (figure 3.1.2) for the evaluation of substrate extraction tools (section 3.2.2 and 3.2.3).

Unlike our 2D FEM model which is a cross sectional representation of the buried layer and the resistive continuum of the substrate, this 3D model includes the complete cross-section of the considered technology. However, no functional devices are placed inside the regions above the buried layers $T0$, $T1$ and $T2$, which in this layout are represented by logic p-wells.

As described in section 2.1, the result from the extraction tools is a circuit representation of the substrate. This circuit representation will also include the buried layer, and for this simulation the substrate height h is chosen to be 300 µm. In simulating the Y-parameters of this circuit and connecting the appropriate negative capacitors to $T0$, $T1$ and $T2$, we are able to obtain the same resistor representation as the bare substrate of our parasitic substrate model. The basis of our evaluation is then the extent to which resistors we obtained from our 2D FEM model match the ones produced by the extraction tools. For this comparison we will convert the 2D resistors appropriately to our 3D model. Table 3.2.1 shows how each 2D resistor is converted.

R $[\Omega\mu m]$	R′ $[\Omega]$
R0B	$\mathrm{R0B}\frac{1}{8g}$
R1B	$\mathrm{R1B}\frac{1}{4g}$
R2B	$\mathrm{R2B}\frac{1}{l}$
RTB	$\mathrm{RTB}\frac{1}{12(g+l)-4l}$
R0T	$\mathrm{R0T}\frac{1}{8g}$
R1T	$\mathrm{R2T}\frac{1}{4g}$
R2T	$\mathrm{R2T}\frac{1}{4l}$
R01	$\mathrm{R01}\frac{1}{4(g+l)}$
R12	$\mathrm{R12}\frac{1}{l}$
R02	$\mathrm{R02}\frac{1}{2g}$

Table 3.2.1: Conversion rates for the resistor values obtained from the 2D FEM model (figure 3.1.2) to the 3D test layout illustrated in figure 3.2.1.

3.2.2 Substrate extraction using Quantus QRC Solution

Quantus QRC is the parasitic extraction tool by Cadence. QRC is fully integrated in the design flow environment Virtuoso, and is commonly used in the IC creation process by designers that use Virtuoso. For an accurate extraction of parasitics of a design using a particular semiconductor technology an appropriate configuration is required. However, the methodology of this configuration, which comprises of the creation of a kind of program and configuration file for calibre and QRC, called a *runset*, is very complex and therefore requires dedicated testing. Since QRC is proprietary software, not all details are disclosed, which further complicates the development of a runset.

QRC features metal layer extraction as well as substrate extraction. Whereas the former component is frequently used by all designers, the latter software component is far less frequently used, and, according to Cadence, more of a niche application.

Over the years the runsets for each technology have been optimized. Runsets for the substrate extraction of the technology we analyze have been developed, however, they are not considered to be extensively tested for EMC-applications. As we will see in the following, the results we obtain from QRC are for the most part not in agreement with our FEM data. However, from comparing the results with our 2D data, we hope our group can gain some insight as to how to better approach an adequate configuration for the substrate extraction. A full analysis of the results however is beyond the scope of this work. Here, we will merely compare the results we obtained from two different ways of configurating QRC.

An essential part of the configuration of QRC is to specify the devices of the layout that are connected to the substrate. Each such device that is passed to QRC for substrate extraction is associated with a "seed polygon". The shape and position of the seed layer polygon, together with the QRC runset, defines how and where the device is connected to the substrate continuum. In addition, QRC can also be configured to produce continuum models of wells, and direct connections to the metal interconnect [17, 18]. The well-feature of QRC has not been used to describe the N-buried layer, albeit we think that this would yield more accurate results than our current approach, which is to contain the whole n-buried layer in the device model, because we think this considerably reduces the size of the resulting netlist.

The two types of configurations we examine are illustrated in figure 3.2.2. In the first

case, the n-buried layer to substrate junctions are partitioned by area among multiple devices – one for each n-sinker. In the second case, each n-epi pocket is only associated with one device, which represents the complete junction.

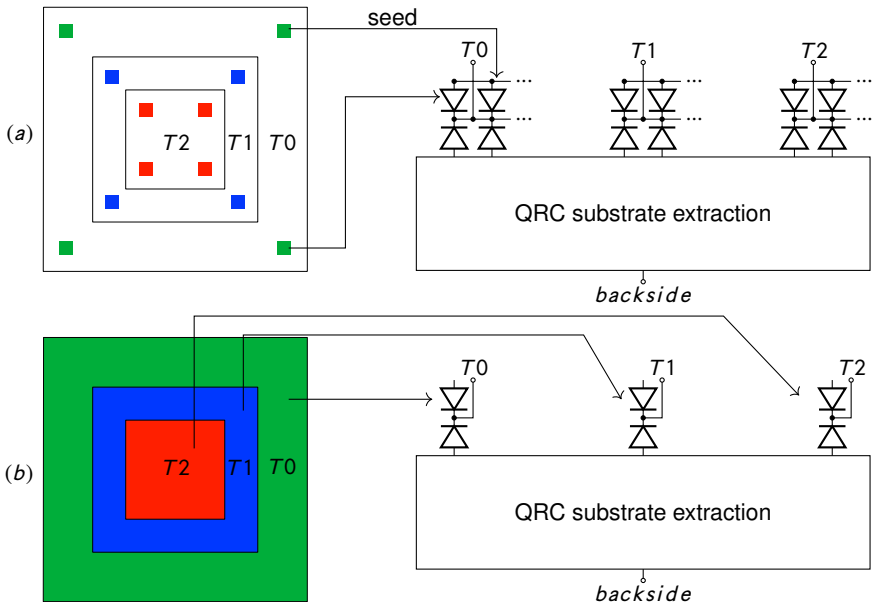


Figure 3.2.2: Illustration of the two different configuration methods used for the QRC substrate extraction (trenches not depicted).

We will try to draw some conclusions on how these two different configurations affect the substrate extraction made by QRC. For this, we compare the results we obtain for the resistors R0B, R1B, and R2B for $d_1 = 50\,\mu\text{m}$ and $d_2 = 400\,\mu\text{m}$ at $f = 1\,\text{GHz}$. The results are listed in table 3.2.2.

Simulation	$\frac{1}{\text{R0B}}\left[\frac{1}{\Omega}\right]$		$\frac{1}{\text{R1B}}\left[\frac{1}{\Omega}\right]$		$\frac{1}{\text{R2B}}\left[\frac{1}{\Omega}\right]$	
	d_1	d_2	d_1	d_2	d_1	d_2
FEM	3.4	3.8	2.7×10^{-2}	2.6×10^{-1}	4.2×10^{-1}	4.2×10^{-1}
QRC (*a*)	0.041	0.052	4.0×10^{-4}	1.2×10^{-4}	2.0×10^{-3}	1.1×10^{-3}
QRC (*b*)	1.7[a]	1.8[a]	9.8×10^{-5}	1.6×10^{-4}	7.7×10^{-5}	7.5×10^{-5}

for $f = 1\,\text{GHz}$
$d_1 = 50\,\mu\text{m}$
$d_2 = 400\,\mu\text{m}$
[a] smallest deviations from FEM data

Table 3.2.2: Comparison of the resistor values R0B, R1B and R2B obtained from the QRC substrate extraction with the converted (see table 3.2.1) results from the 2D FEM simulation.

Although none of the results in table 3.2.2 reasonably match match our FEM data, and most of them deviate by at least a factor of 10^2, we can draw some conclusions regarding the effects on the QRC substrate extraction using configurations (*a*) and (*b*). We have observed for different d that the resistor value for R0B we obtain from configuration (*b*) is with respect

to the values for R1B and R2B (deviation by ca. four orders of magnitude) in better agreement (deviation within ca. 9dB) with the FEM results. On the other hand the resistor values we obtain from configuration (*a*) all show a deviation by ca. two orders of magnitude. This clearly shows that the size of the seed polygon matters a lot, and that larger seed polygons yield better results.

For another, we observe that in configuration (*b*) the shapes of $T0$ and $T1$ are toroidal whereas the shape of $T2$ is represented by a rectangle, a simpler geometry. It is unclear why for different d[5] the result for R0B is in better agreement (see ^{a} in table 3.2.2) with the FEM data than R1B and R2B, yet we can deduce that the geometrical shape that represents the connection area is most likely not a deciding factor.

3.2.3 SUBEX substrate extraction

In this section we will evaluate an in-house substrate extraction tool, code-named "SUBEX", that is currently under development. As mentioned in section 3.2.2, the configuration methods of the QRC substrate extraction tool are very complex, and since some details of its methodology are undisclosed, an adequate configuration is aggravated. In this respect, the usage of an internally developed substrate extraction tool has a clear advantage. Furthermore, SUBEX uses an FEM based extraction technique and a special model reduction technique which strongly reduces the 3D FEM discretized Laplace's equation. As a consequence, SUBEX is capable to produce parasitic substrate netlists that are both well performing in circuit simulators and accurate [19].

The following evaluation of this tool will be kept brief, and only intends to convey a basic idea of the accuracy that can be expected from this tool. An extensive analysis of SUBEX can be found in [3]. For our evaluation we will compare the results we obtained for the resitor R02 with our 2D FEM data.

In figure 3.2.3 results for frequencies $f \in \{1\,\text{MHz}, 1\,\text{MHz}\}$ and distances $d \in \{50\,\mu\text{m}$, $100\,\mu\text{m}$, $200\,\mu\text{m}$, $400\,\mu\text{m}$, $800\,\mu\text{m}\}$ are illustrated. These results show, for the most part, an excellent agreement with our 2D FEM data. The largest deviation of the magnitude of 1/R02 is approximately 5dB. Deviations regarding the phase of 1/R02 are below 45°. Moreover, the zero crossing of the magnitude of 1/R02 is observed for a similar value for d as in our FEM results. Since the conversion of the 2D FEM values for the resistor R02 are not an exact representation of that in our 3D model (figure 3.2.1), the conversion partly accounts for these discrepancies. At this point we cannot make any assumptions as to the magnitude of the 2D to 3D conversion error, and to further pin down the causes for these deviation would require a more extensive analysis which however is beyond the scope of this work.

To further examine the impact of the special model reduction algorithm that SUBEX uses we have also simulated the initial FEM discretized substrate which has not yet been modified by this technique. We have observed that the simulation times of the reduced substrate netlists were significantly shorter. The impact on accuracy by the size reduction of the substrate netlists on the other hand is negligible, as can be seen in the plots we provide in the appendix (figures A.3.1 and A.3.2).

[5] We have also observed this for $d \in \{100\,\mu\text{m}, 200\,\mu\text{m}\}$

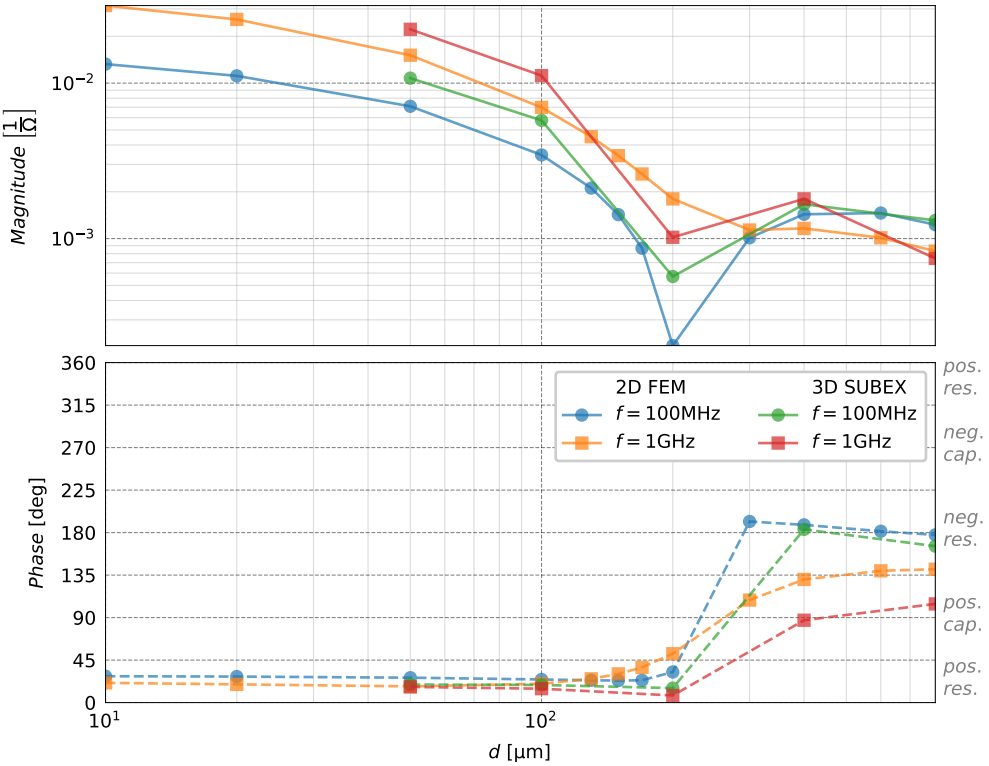


Figure 3.2.3: Comparison of the 2D FEM and SUBEX extraction results of the distance dependance of the magnitude and phase of R02^{-1} for different frequencies.

4 Concluding Remarks

Our main goal comprised of the creation of a low dimensional parasitic substrate circuit capable of modelling substrate couplings between two adjacent devices on a die. An important feature of this model was to describe each capacitive layer of the pn-jucntion underneath a device by a single capacitor. For this to be possible we found, from the results of a 2D FEM simulation of the substrate model described in section 3.1.1, that the values of some of the resistors in our parasitic substrate circuit have to be dependant on frequency. Moreover, from the results in sections 3.1.4 and 3.1.5 we were able to constrain the domain of d to $d \leq 200\,\mu\text{m}$ for which our parasitic substrate circuit can be used for obtaining adequate predictions for substrate couplings. For $d > 200\,\mu\text{m}$ cancellation effects caused by the resistor R02 are too significant to obtain reasonably accurate coupling predictions.

The second goal involved the evaluation of the two substrate extraction tools, QRC and the in-house tool SUBEX, using the results obtained from the 2D FEM simulation. Both tools were tested on a 3D layout (figure 3.2.1) comparable to the 2D FEM model (figure 3.1.2). The evaluation of QRC yielded some important findings to be used for its appropriate configuration. In the evaluation of SUBEX we found an excellent agreement of the extraction results with the 2D FEM data which points to a strong reliability of this tool.

A Additional Plots

A.1 Additional 2D FEM resistor data

R02 Additional data for the resistor R02 of the parasitic substrate circuit (figure 3.1.4).

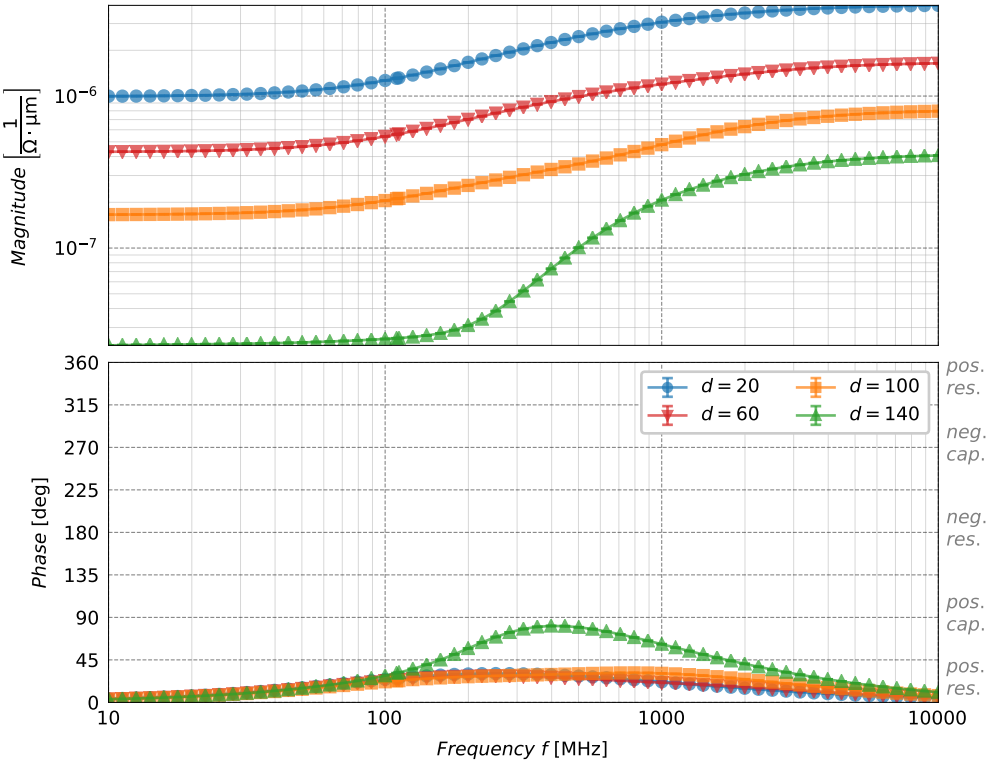


Figure A.1.1: Frequency dependance of the magnitude and phase of $R02^{-1}$ for small values of d.

R0T, R2T Additional data for the resistors R0T and R2T.

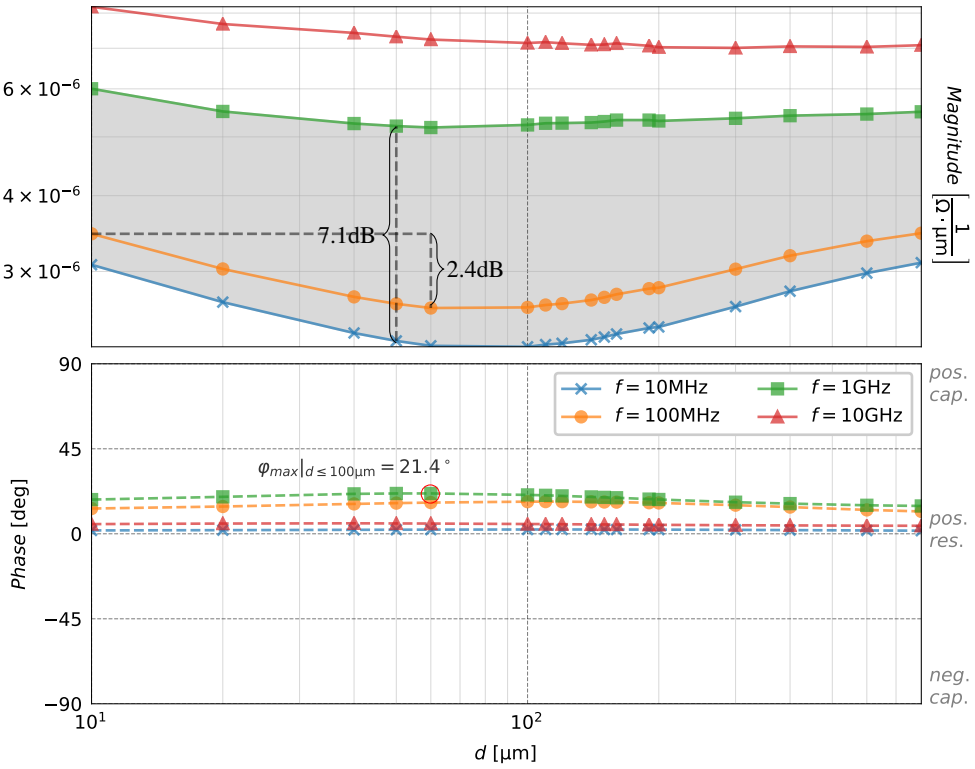


Figure A.1.2: Distance dependance of the magnitude and phase of $R0T^{-1}$ and $R2T^{-1}$ for different frequencies.

R0B, R2B Additional data for the resistors R0B and R2B.

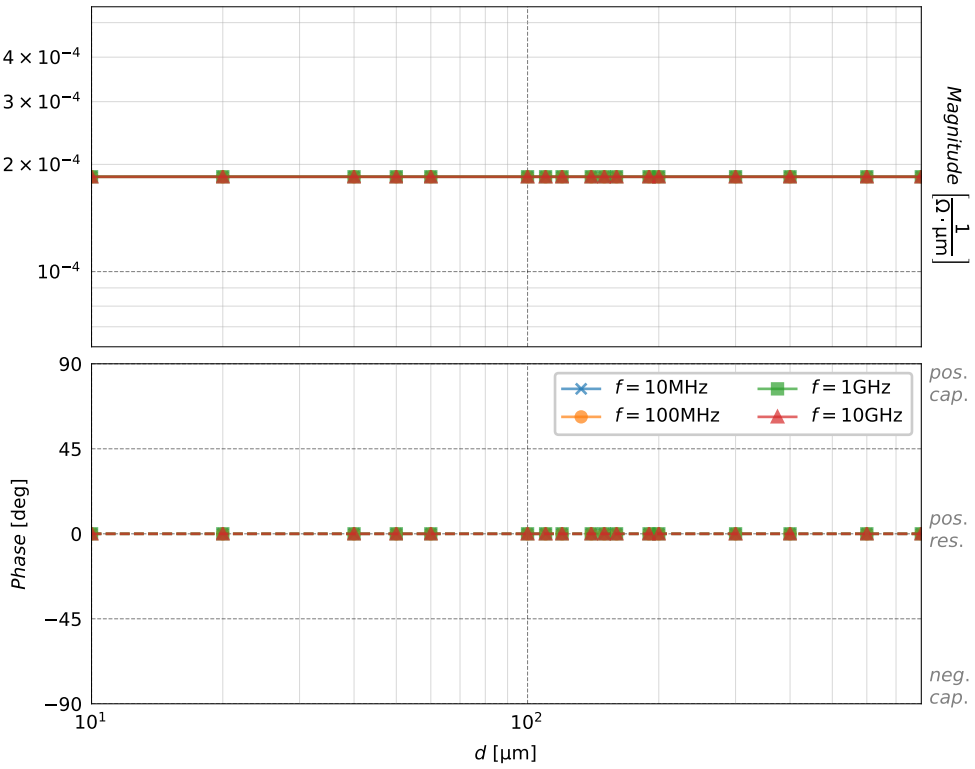


Figure A.1.3: Distance dependance of the magnitude and phase of $R0B^{-1}$ and $R2B^{-1}$ for different frequencies.

R1B Additional data for the resistor R1B:

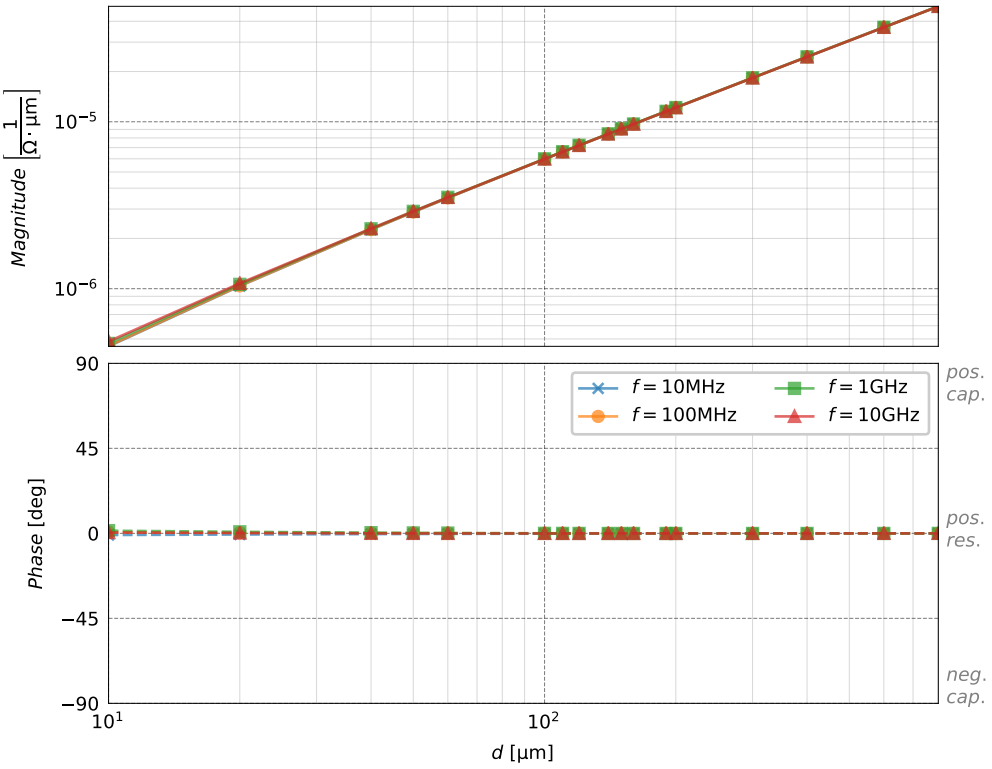


Figure A.1.4: Distance dependance of the magnitude and phase of $R1B^{-1}$ for different frequencies.

RTB Additional data for the resistor RTB:

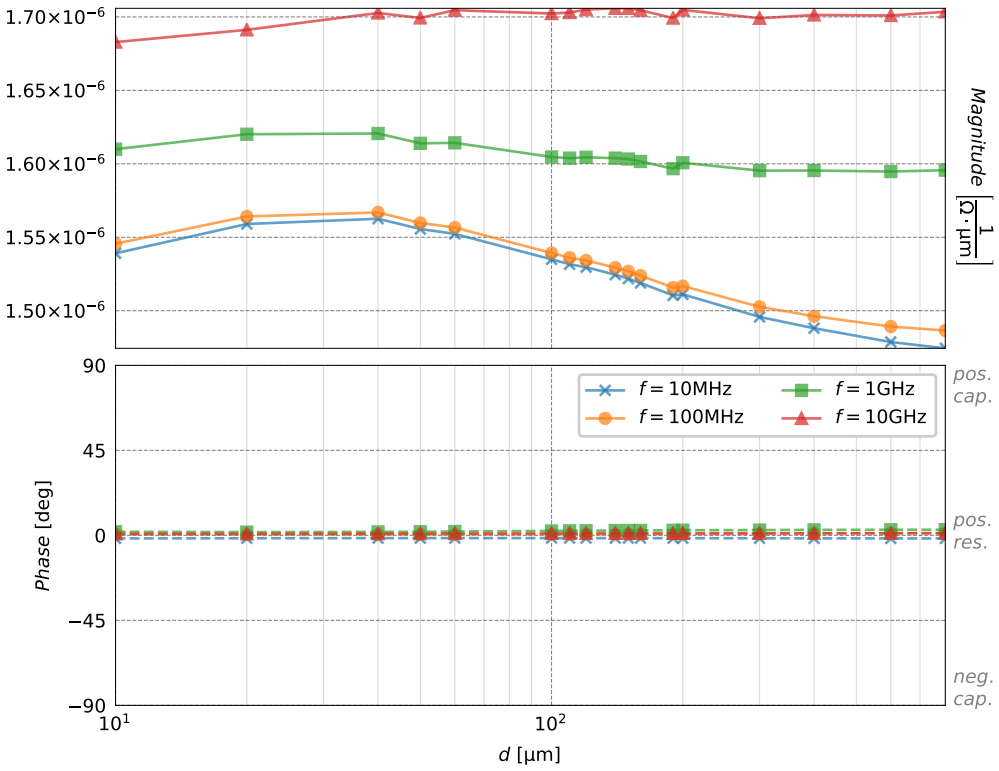


Figure A.1.5: Distance dependance of the magnitude and phase of RTB^{-1} for different frequencies.

A.2 Field plots

The field plots shown here depict the current density J normalized by $\bar{V}_{T2}$, the average voltage on the substrate surface region $T2$ for an AC-voltage excitation at $T2$. The magnitude of $\frac{J}{\bar{V}_{T2}}$ is illustrated by colors, the values of which can be obtained by comparing the colorbar in figure A.2.1. The current direction is indicated by the black ellipses which represent a full period, and the zero phase is indicated by a red line. Note the frequency dependance of the shapes of these ellipses.

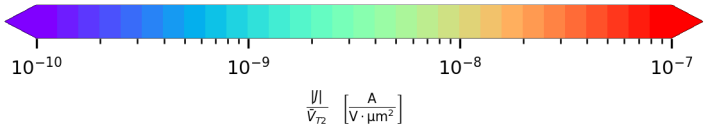


Figure A.2.1: color bar for figures ref1 and ref2

Large distances Field plots for distances $d = 160\mu m$ and $d = 600\mu m$

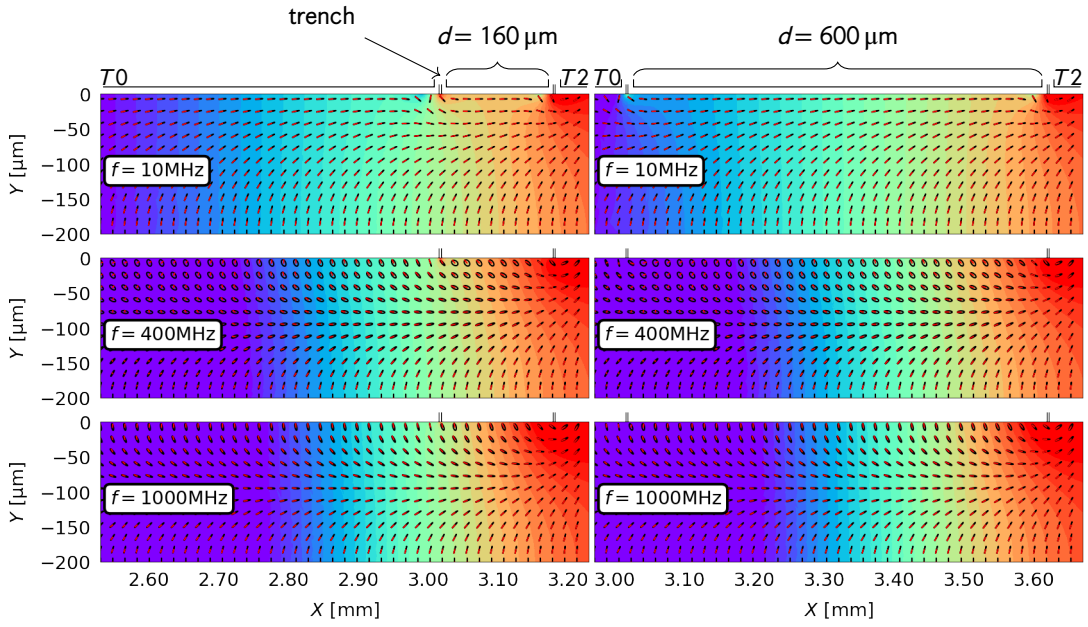


Figure A.2.2: Box plot of number of positions sent per iteration using this scheme

Small distances Field plots for distances $d = 20\mu m$ and $d = 140\mu m$

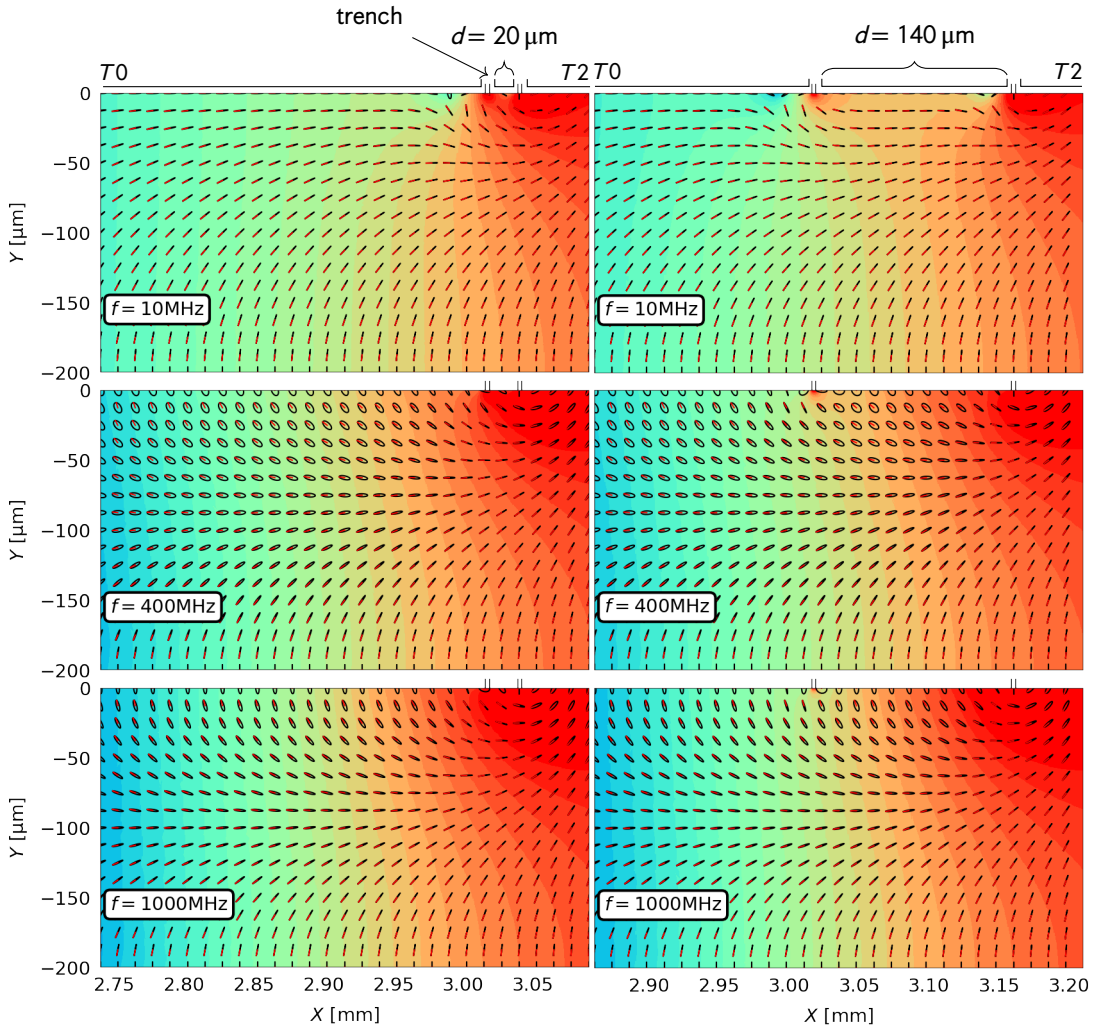


Figure A.2.3: Box plot of number of positions sent per iteration using this scheme

A.3 SUBEX

Compared here are some frequency dependant data we obtained for the resistor R02 from the Y-parameter simulation of (*a*), the "raw" FEM netlist which is subject to the special model reduction technique and (*b*), the netlist resulting from the reduction.

Small distance Frequency dependance for $d = 50\,\mu\text{m}$

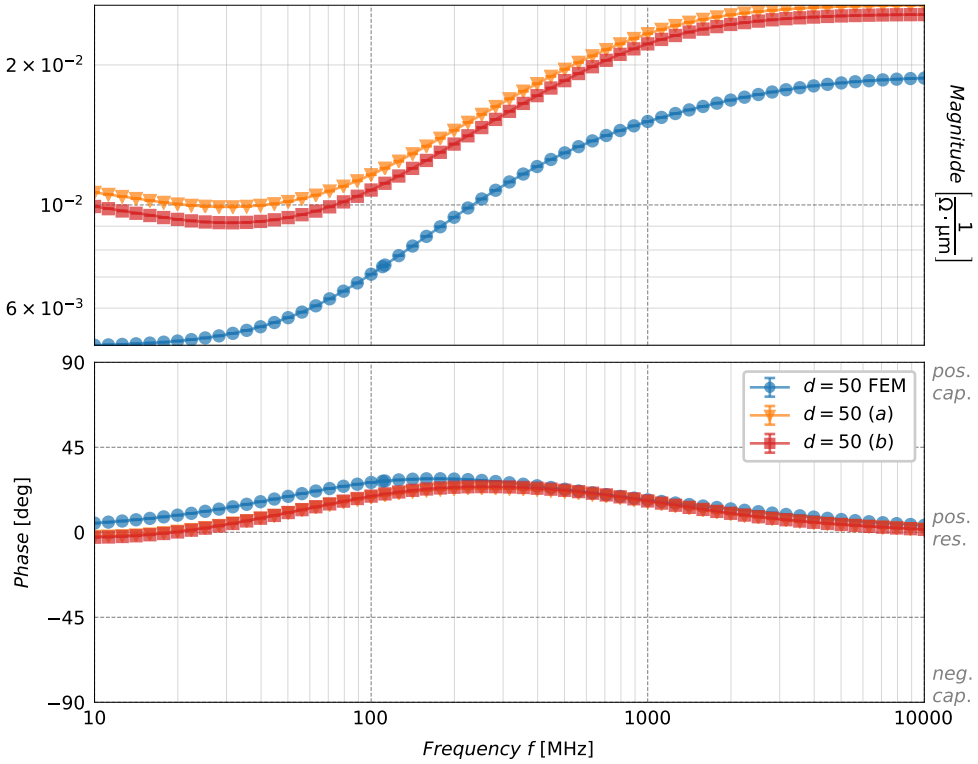


Figure A.3.1: Frequency dependance of the magnitude and phase of R02^{-1} for $d = 50\,\mu\text{m}$. Blue graph shows the value obtained from the 2D FEM simulation model.

Large distance Frequency dependance for $d = 400\,\mu\text{m}$

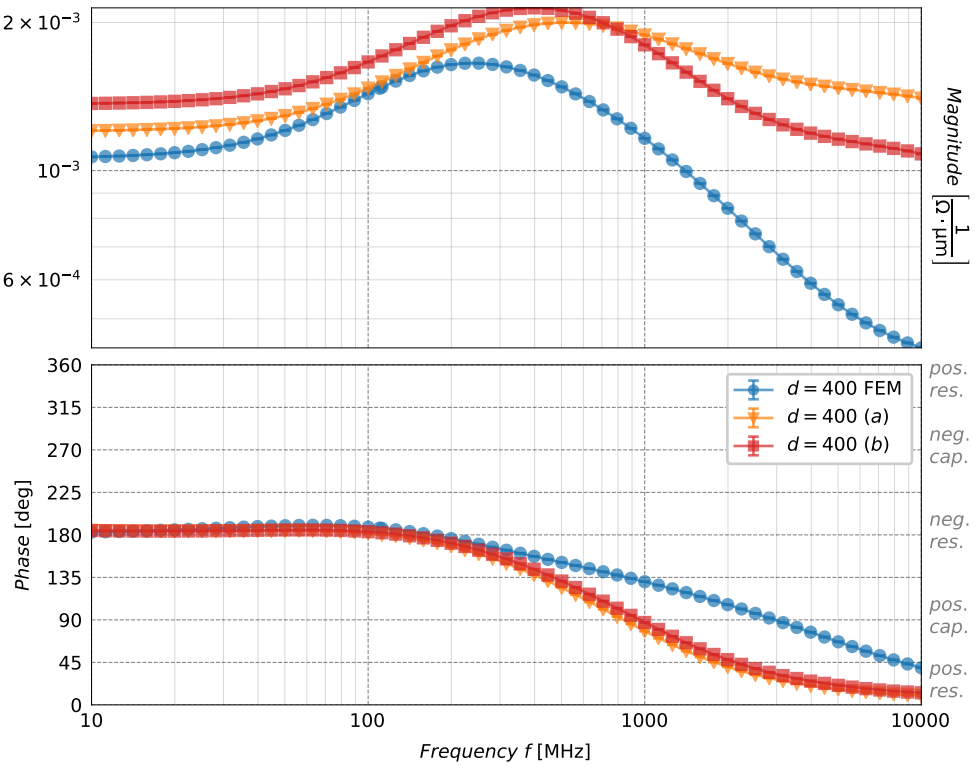


Figure A.3.2: Frequency dependance of the magnitude and phase of R02^{-1} for $d = 400\,\mu\text{m}$. Blue graph shows the value obtained from the 2D FEM simulation model.

References

[1] Ali Keyhani et al. *Handbook of Automotive Power Electronics and Motor Drives*. 1st ed. CRC Press, Taylor & Francis Group, 2005.

[2] *Semiconductors – Technical information and characteristics data*. 2nd ed. revised and considerably enlarged. Publicis Corporate Publishing, 2004.

[3] Alexander Schade et al. 'Modellierung und Messung von Emissionen aus Transceiverpins in Automotive System ICs verursacht durch integrierte DC/DC-Wandler (German)'. In: *EMV* (2020).

[4] *TLE9273QC Data Sheet*. Rev. 1.5. High-End System Basis Chip. Infineon Technologies AG. 2019.

[5] *TLF35584 Data Sheet*. Rev. 1.0. Infineon Technologies AG. 2019.

[6] *LIN Specification Package*. 2.2A. LIN Consortium. 2010.

[7] A.Vladimirescu et al. *SPICE Version 2G User s Guide*. Department of Electrical Engineering and Computer Sciences, University of California, 2020. URL: `http://www.eecg.toronto.edu/~kphang/teaching/spice/index.html` (visited on 01/03/2020).

[8] Ricardo Martins, Nuno Lourenco and Nuno Horta. *Analog Integrated Circuit Design Automation*. 1st ed. Springer, 2017.

[9] Philip E. Allen and Douglas R. Holberg. *CMOS Analog Circuit Design*. 2nd ed. international. Oxford University Press, 2010.

[10] Stuart K. Tewksbury and Joe E. Brewer. *CMOS – circuit design, layout and simulation*. 2nd ed. revised. IEEE Press Series on Microelectronic Systems, 2008.

[11] Jan Albers. *Grundlagen integrierter Schaltungen – Bauelemente und Mikrostrukturierungen (German)*. 1st ed. Hanser, 2006.

[12] *Ansys Electronics Desktop Documentation*. Ansys, Inc. 2020.

[13] Horst Clausert et al. *Grundgebiete der Elektrotechnik 2 (German)*. 10th ed. Oldenbourg, 1980.

[14] David M. Pozar et al. *Microwave Engineering*. 4th ed. John Wiley & Sons, Inc., 1980.

[15] Gunnar Filipsson. 'A New General Computer Algorithm for S-Matrix Calculation of Interconnected Multiports'. In: *1981 11th European Microwave Conference* (1981).

[16] Piero Triverio. *Vector Fitting*. 2019. URL: `https://arxiv.org/pdf/1908.08977.pdf` (visited on 01/03/2020).

[17] *QRC Extraction Users Manual*. Cadence Design Systems, Inc. 2019.

[18] *QRC Techgen Reference Manual*. Cadence Design Systems, Inc. 2019.

[19] Alexander Schade et al. 'S-EHRFEM – Substrate Extraction using Highly Reduced FEM-meshes for Transient SPICE-simulation with Iterative Linear Solvers'. In: *2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE* (2019).